Photovoltaic Equipment

International Technology Roadmap for Photovoltaic (ITRPV)

2019 Results

Eleventh Edition, April 2020

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Content

1. Executive Summary

The photovoltaic (PV) industry needs to provide power generation products that can compete with both, conventional energy sources and other renewable sources of energy. An international technology roadmap can help to identify trends and to define requirements for any necessary improvements. The aim of the International Technology Roadmap for Photovoltaic (ITRPV) is to inform suppliers and customers about anticipated technology trends in the crystalline silicon (c-Si) based photovoltaic industry and to stimulate discussion on required improvements and standards. The objective of the roadmap is not to recommend detailed technical solutions for identified areas in need of improvement, but instead to emphasize to the PV community the need for improvement, to formulate requirements to meet in the future and to encourage in this way the development of comprehensive solutions. The present, eleventh edition of the ITRPV was jointly prepared by 57 leading international poly-Si producers, wafer suppliers, c-Si solar cell manufacturers, module manufacturers, PV equipment suppliers, and production material providers, as well as PV research institutes and consultants. The present publication covers the entire c-Si PV value chain from crystallization, wafering, cell manufacturing to module manufacturing, and PV systems. Significant parameters set out in earlier editions are reviewed along with several new ones, and discussions about emerging trends in the PV industry are reported.

The global c-Si cell and PV module production capacity at the end of 2019 is assumed to have further increased to about 200 GWp due to continued PERC capacity expansions [1, 2, 3]; the market share of about 95% for the c-Si and about 5% for thin-film technologies is assumed to be unchanged [4].

The PV module market in 2019 increased by about 20% to 130 GWp. The c-Si module market shifted significantly to mono-Si based products. The increased mono-Si wafer and cell capacity resulted in price reductions for mono-Si and a significant price decline for multi crystalline-Si (mc-Si) based products. The weighted average price of c-Si modules stayed quite stable.

A consequent implementation of PERC and other improvements like half-cell interconnect but also the use of larger wafers resulted in higher average module powers. The PV manufacturers installed new PERC cell and module production capacities, capable for new cell formats and upgraded existing production lines to increase cell efficiencies and to enable the use of slightly larger cell formats. The price experience curve continued with its historic learning with a further increase to 23.5%. The PV industry can keep this learning rate up over the next years by continuing the linking of cost reduction measures with the implementation of cell perfections, with improved wafer material, improved cell front and rear sides, refined layouts, introduction of bifacial cell concepts, and improved module technologies. The introduction of larger cell formats will contribute to reduce PV system costs. Improvements in all fields will result in module area efficiency increase: today's main stream p-type mono-Si based modules reach efficiencies of about 20% that will increase to 22.5% within the next 10 years, mc-Si based technologies are expected to improve from today 18.5% to above 20% until 2024. The n-type based module efficiencies will lead the market for highest power modules from today's 20.5% up to 23% within the next 10 years. Heterojunction (HJT) based products will reach module efficiencies close to 24% until 2030. The combination of reduced manufacturing costs and increased cell and module performance will support the reduction of PV system costs and thus ensure the long-term competitiveness of PV power generation. All aspects are again discussed in this revision of the ITRPV.

VDMA continues the Roadmap activity, and updated information will be published annually to ensure comprehensive communication between manufacturers and suppliers throughout the value chain. More information is available at itrpv.vdma.org.

2. Approach

The main c-Si technology value chain elements wafer, cell, and module are discussed in three areas: materials, processes, and products. Data was collected from the participating companies and processed anonymously by VDMA. The participating companies jointly agreed that the results are reported in this roadmap publication. All plotted data points of the parameters reported are median values generated from the input data. Beside the discussion of parameters linked to crystallization, wafers, cells, modules, we look at the impact and trends for PV systems and discuss trends in smart fab manufacturing.

2.1.Materials

The requirements and trends concerning raw materials and consumables used for wafer, cell, and module manufacturing are described in these subsections. Reducing the consumption or substitution of some materials will be necessary in order to ensure availability, avoid environmental risks, reduce costs, and increase efficiency. Price development plays a major role in making PV-generated electricity competitive with other renewable and fossil sources of energy.

2.2.Processes

New technologies and materials, and highly productive manufacturing equipment are required to reduce production costs. By providing information on key production technologies, as well as details about processes parameters to optimize the wafer production, increase cell and module efficiency as well as module power output, this roadmap constitutes a guide to new developments and aims to support their progress. The subsections on processes identify manufacturing and technology issues for each segment of the value chain. Manufacturing topics center on raising productivity, while technological developments aim to ensure higher cell and module efficiencies.

2.3.Products

Each PV value chain element contributes to final products. The products subsections therefore discuss the anticipated development of the value chain elements ingot, wafer, c-Si solar cells, and module over the coming years.

3. PV Learning Curve

It is obvious that cost reductions in PV production processes will also result in price reductions [5]. Fig. 1 shows the price experience curve for PV modules, displaying the average module sales prices - at the end of the corresponding time period - (in 2019 US$/Wp) as a function of cumulative module shipments from 1976 to 12/2019 (in MWp) [6, 7, 8, 9]. Displayed on a log-log scale, the plot changes to an approximately linear line until the shipment value of 3.1 GWp (shipments at the end of 2003), despite bends at around 100 MWp. This indicates that for every doubling of cumulative PV module shipment, the average selling price decreases according to the learning rate (LR). Considering all data points from 1976 until 2019 we found an LR of about 23.5% - a slight increase compared to the 23.2% in the 10th edition. The large deviations from this LR plot in Fig. 1 are caused by tremendous market fluctuations between 2003 and 2012 as well as in 2016 and 2018.

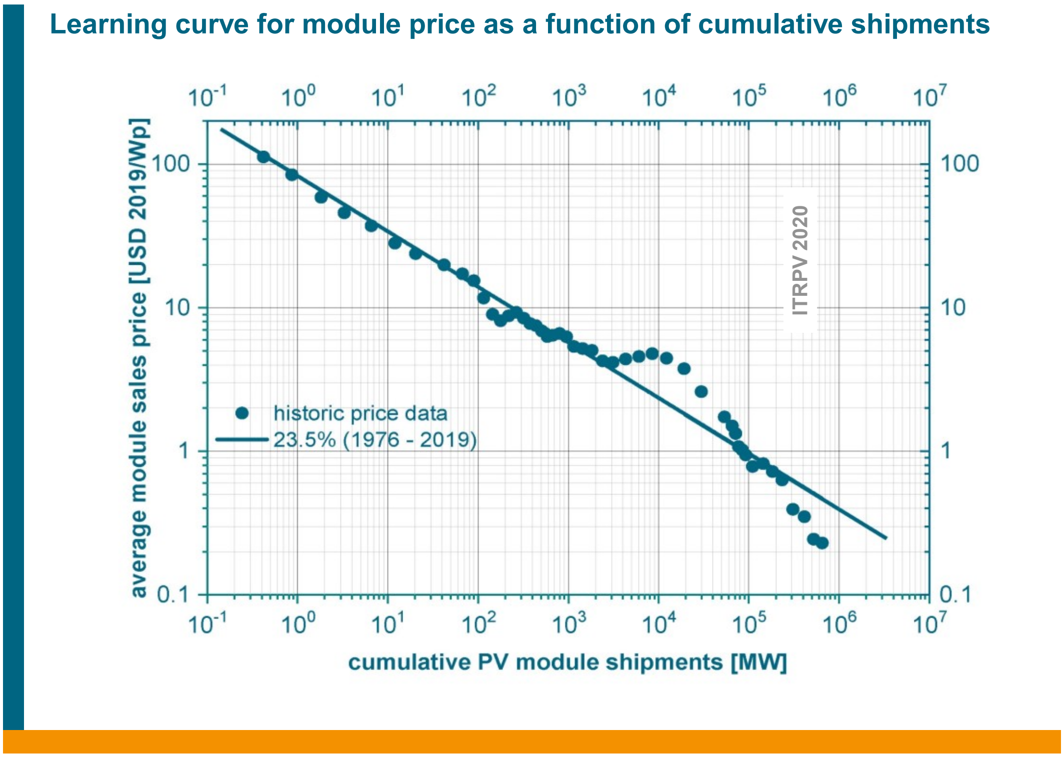

Fig. 1: Learning curve for module spot market price as a function of cumulative PV module shipments.

The last data point indicates the module shipment volume and average spot market price in 2019. The 2019 shipment volume is calculated to 130 GWp - Installation of 123 GWp [7] plus 7 GWp in ware-houses and in transit until year end 2019. Based on this data the cumulated shipped module power at the end of 2019 is calculated to approximately 654 GWp. The resulting worldwide installed cumu-lated module power reached 628 GWp end of 2019 after 505 GWp in 2018 [10]. The corresponding average module spot market price at the end of 2019 is calculated to 0.23 US$/Wp as described in chapter 4.

4. Cost Consideration

Fig. 2 and Fig. 3 show the price development of mono- and mc-Si modules respectively from January 2014 to January 2020 with separate price trends for poly-Si, mono- and mc-Si wafers, cells and modules [9].

Price Trend for mono-Si modules

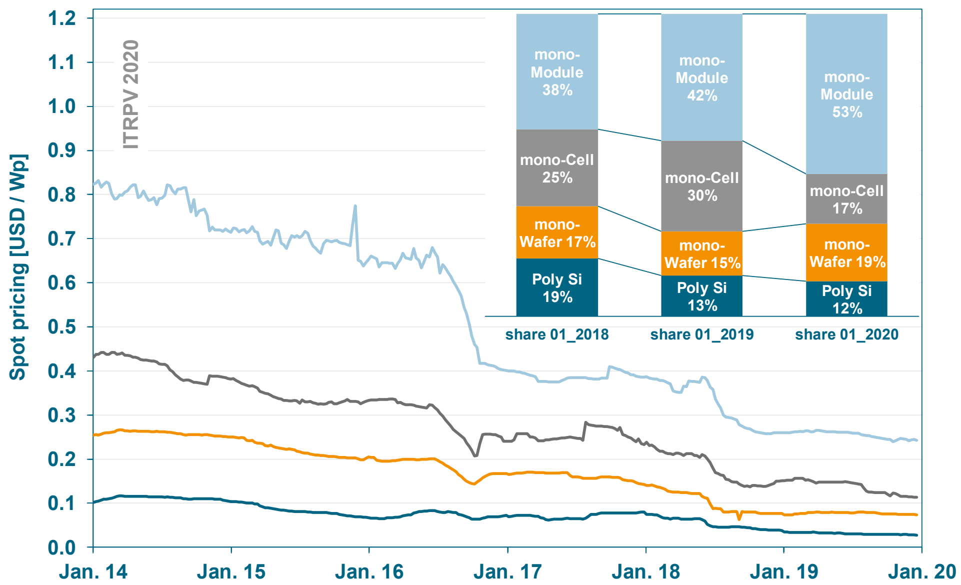

Fig. 2: Spot market price trends for poly-Si, mono-Si wafers, cells, and modules (assumption 01/2020: 15 g poly-Si per mono wafer (Fig. 4), average mono-Si cell efficiency 21.5%, (5.3 Wp); inset: comparison of the proportion of the price attributable to different cost elements between 01/2018, 01/2019, and 01/2020 (0.39, 0.26, and 0.24 US$/Wp) [9].

Module production capacity at the end of 2019 is assumed to be above 200 GWp due to continued capacity expansions [2]. In parallel, the 2019 PV installations in China were with 30 GWp repeatedly lower than in the previous years (44 GWp 2018, 55 GWp 2017) [11].

The spot market price for mono-Si and mc-Si modules respectively fell during 2019 only by about 10% while the corresponding cell prices dropped by 20% in the same time frame. The average module prices are calculated for 01/2018, 01/2019, and 01/2020 for mono-Si modules to 0.39, 0.26, and 0.24 US$/Wp and for mc-Si modules to 0.31, 0.23, and 0.21 US$/Wp respectively [9], We calculated a weighted average price of c-Si modules at year end of 2019 to 0.23 US$/Wp based on the 2019 market share of 65% for mono- and 35% for mc- wafers as shown in Fig. 14.

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The inset of Fig. 2 and Fig. 3 show the comparison of the proportion of prices attributable to silicon, wafer, cell, and module price between January 2018 and January 2020. The overall price level for modules stayed quite stable but the module portion increased to above 50%. While the wafer prices for mono-Si wafers stayed quite stable, prices for mc-Si wafers suffered from a continued price decline mainly due to the shrinking market share.

Prices for mc-Si cells followed this trend and drop by about 25% during 2019. Mono-Si cell prices dropped in 2019 also by 25% in contrast to the stable mono-Si wafer prices. So, we conclude that the increased price portion for the module conversion is caused in a high portion by the introduction of larger wafer formats resulting in higher module powers at the expense of higher material cost for the larger modules.

The non-silicon module manufacturing costs are mainly driven by consumables and materials as discussed in the c-Si PV module cost analysis in the 3rd edition of the ITRPV. Taken into account the fact that the anticipated global PV module production capacity of above 200 GWp in 2019 [2] will further increase in 2020 due to continued capacity expansions, the production capacity will not at all meet the predicted global market demand of ≈142 GWp in 2020 [12] but will again exceed it. Therefore, prices will not compensate for any cost increases as there is no shortage expected - in other words, the pressure on wafer, cell and - more painful - on module manufacturing - will persist unchanged. Achieving cost reductions in consumables, and materials will be more difficult but must be continued. Improving productivity and product performance will stay in the focus resulting in further pressure to older, depreciated manufacturing lines.

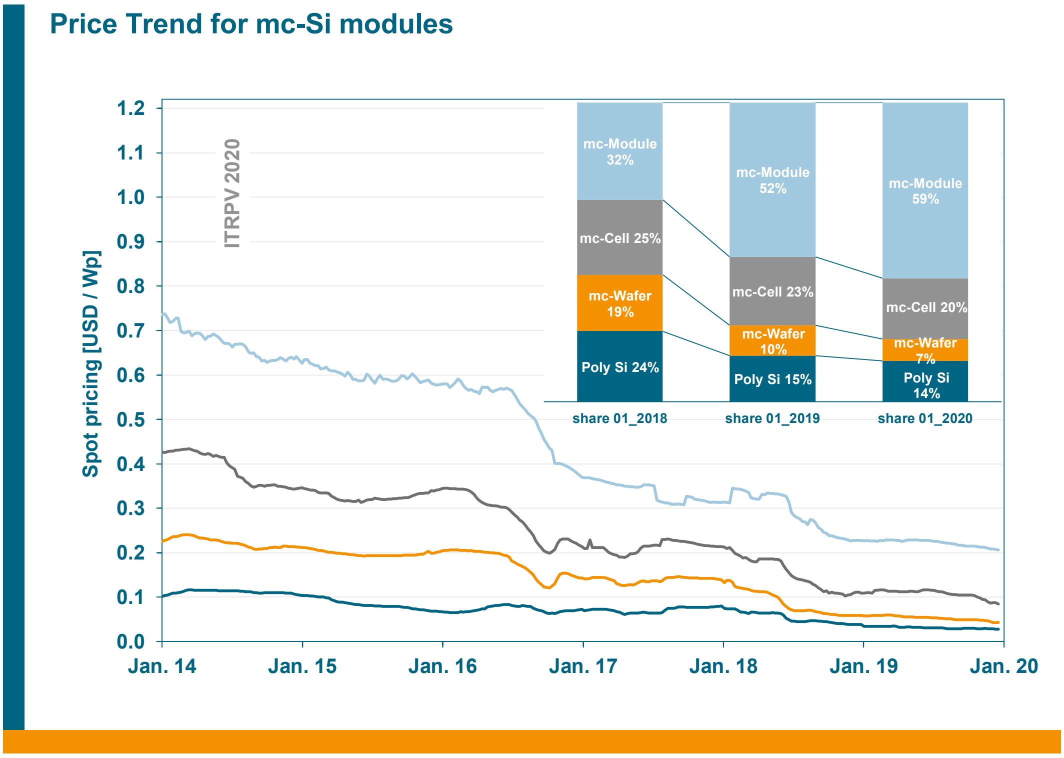


Fig. 3: Spot market price trends for poly-Si, mc-Si wafers, cells, and modules (assumption 01/2020: 16 g poly-Si per wafer (Fig. 4), average mc-Si cell efficiency: 19.8% {4.9 Wp) inset: comparison of the proportion of the price attributable to different cost elements between 01/2018, 01/2019, and 01/2020 (0.31, 0.23, and 0.21 US$/Wp) [9].

The known three strategies, emphasized in former ITRPV editions help to address this challenge:

- Improve module area efficiency without significantly increasing the processing cost.
- Continue the cost optimization per piece along the entire value chain by increasing the Overall Equipment Efficiency (OEE) of the installed production capacity, by using Si and non-Si materials more efficiently, and enabling higher OEE of new installed capacities.
- Introduce specialized module products for different market applications (i.e. tradeoff between cost-optimized, highest volume products and highest efficiency, higher price roof-top applications or even fully customized niche products).

The first point implies that cell efficiency improvements need to be implemented in parallel with new module concepts to improve the module area efficiency. To enable cost efficient manufacturing this must be implemented with lean processes to optimize capital expenditures. It will remain difficult to introduce new, immature technologies that do not show reductions of the cost per Wp from the beginning. Nevertheless, the Toprunner Program in China continues the motivation to meet these challenges [13, 14]

5. Results of 2019 | Crystallization and Wafering

5.1. Materials

With about 15% price share, poly-Si remains the most expensive material of a c-Si solar cell as discussed in chapter 4. Siemens and FBR (Fluidized Bed Reactor) processes remain the main technologies to produce poly-Si. Today, FBR processing has a share of < 5% and we expect that its share will not increase significantly against the well matured and further optimized Siemens process [15]. Other technologies like umg-Si (upgraded metallurgical grade-Si) are not expected to yield significant cost advantages compared to matured poly-Si technologies over the coming years, but are expected to stay available in the market.

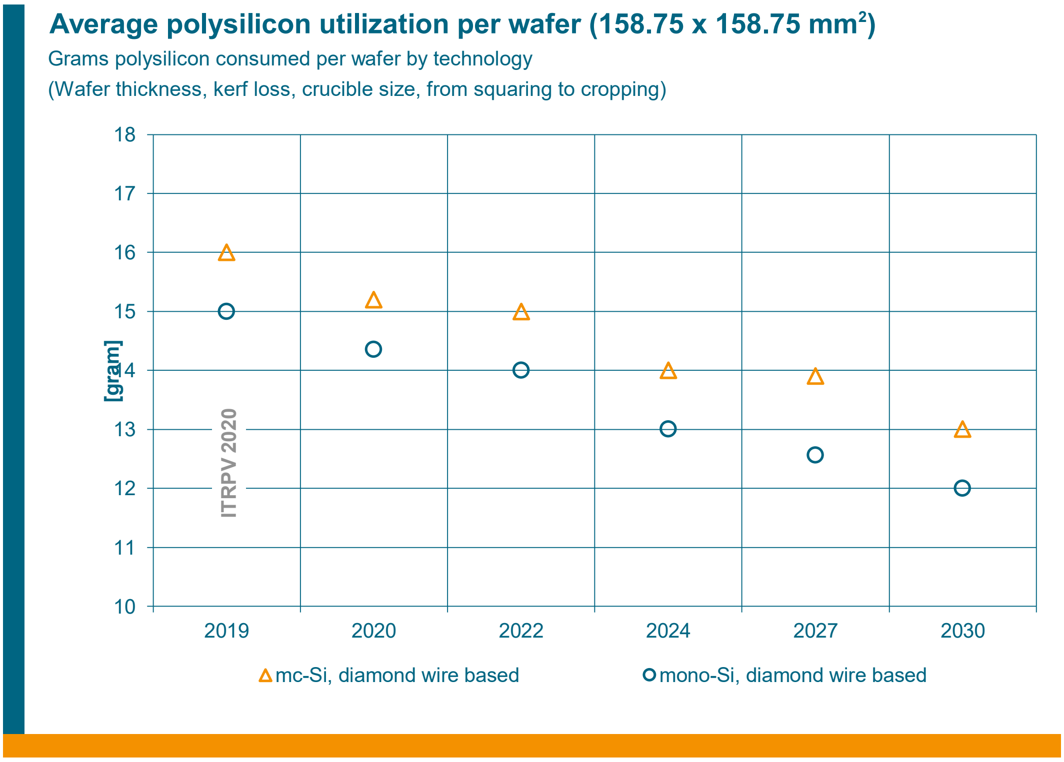


Fig. 4: Average polysilicon consumption for mc-Si and mono-Si wafers with diamond wafer sawing technology.

Fig. 4 shows the average utilization of poly-Si to produce silicon wafers. The weight of a 180 µm 158.75 mm x 158.75 mm mono-Si or mc-Si wafer is about 9.7 g. 15 g or close to 150% of remaining Si was used in 2019 to produce a standard mono-Si wafer. Mc-Si wafers consume about 7% more poly-Si than mono-Si wafers. We expect that the poly-Si usage will be improved further during the next years.

5.2.Processes

5.2.1. Crystallization

It is possible to increase the throughput of the crystallization process by changing the common sizes of the ingots and by growing more crystals with the same crucible. Fig. 5 shows the increase of ingot mass for casted silicon materials and for Czochralski (Cz) growth of mono-Si, as predicted by the roadmap. Gen 8 ingoting is becoming mainstream with ingot masses of 1100 kg in 2019 and up to 1200 kg in 2024. Casted ingot mass will move to Gen 9+ after 2027 and increase further towards 1600 kg. The mass of cast-mono-Si ingots is expected to increase as well but slower, while the ingot mass of mono-Si is expected to increase continuously within the next 10 years. Cz growth will remain the main method for growing mono-Si ingots. Continuous Czochralski (CCz), recharging and multi pulling are expected to contribute to a better use of consumables during the crystallization process. Special crystallization methods like Float Zone (FZ) or magnetic CZ to reduce oxygen content are expected to have no considerable market share over classical Cz, especially if gallium doping will be used in future.

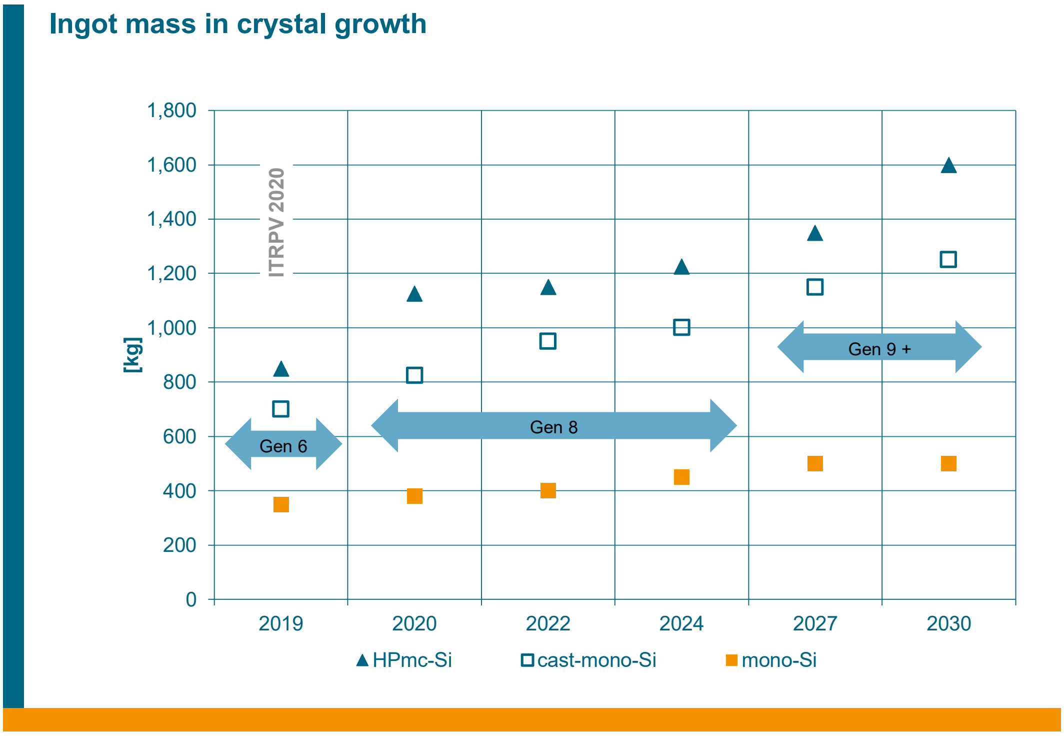


Fig. 5: Predicted trend for ingot mass for mc-Si and for mono-Si.

We asked again about the power consumption of crystal growth. Fig. 6 shows that mono-Si ingot growth consumes about four-times more energy per kg than ingot growth by casting. Poly-Si consumption for mono crystallization is expected to be reduced over the next 10 years by about 20%, while the consumption for casting is expected to stay at between 6 kWh/kg and 7 kWh/kg. Power consumption for cast-mono-Si, today about 40% higher than for mc-Si casting, will be reduced to similar power consumption levels as mc-Si casting.

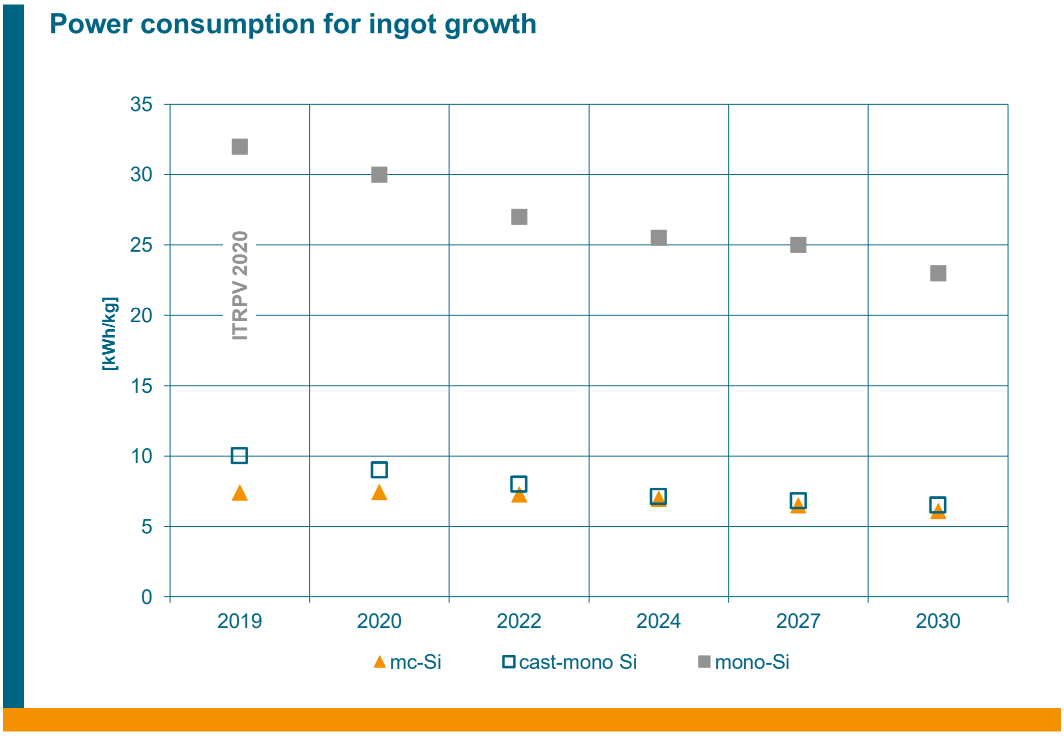


Fig. 6: Trend of power consumption for ingot growth.

Further engineering is done to improve mc-Si material properties despite the shrinking market share. Fig. 7 shows that the share of p-type mc-Si material doped with boron and additional co-doping with Ga and P will increase fast in the next years. This measure improves the material performance for mc-Si PERC due to improved doping homogeneity [16].

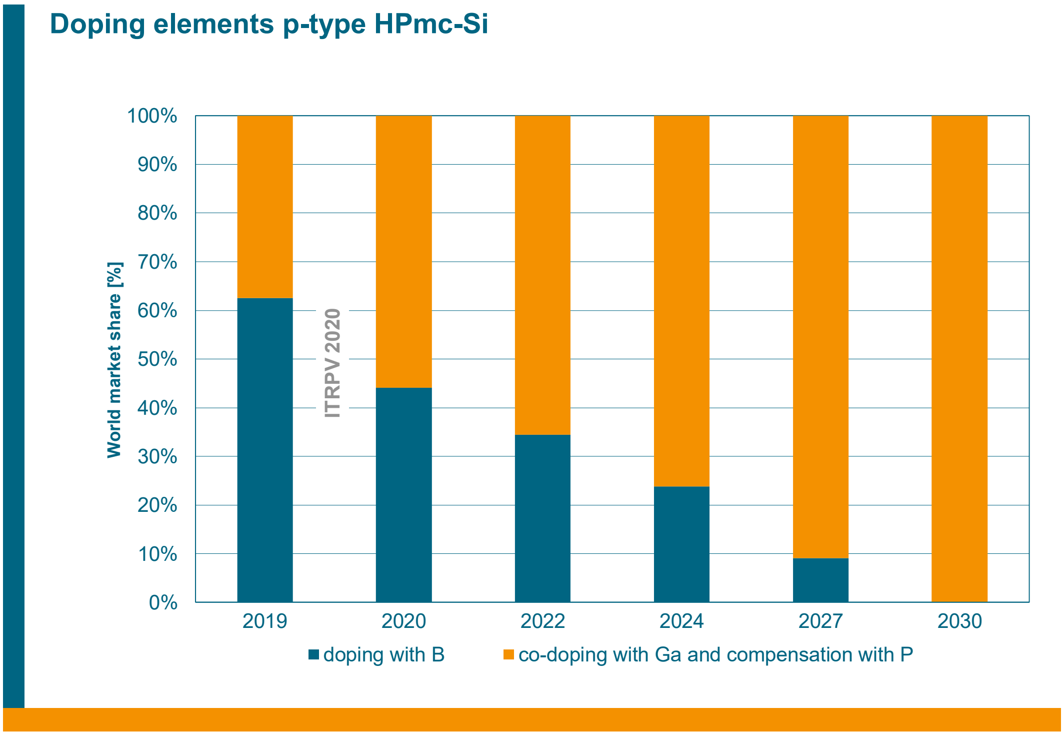


Fig. 7: Expected market share of dopands used for doping of p-type mc-Si material.

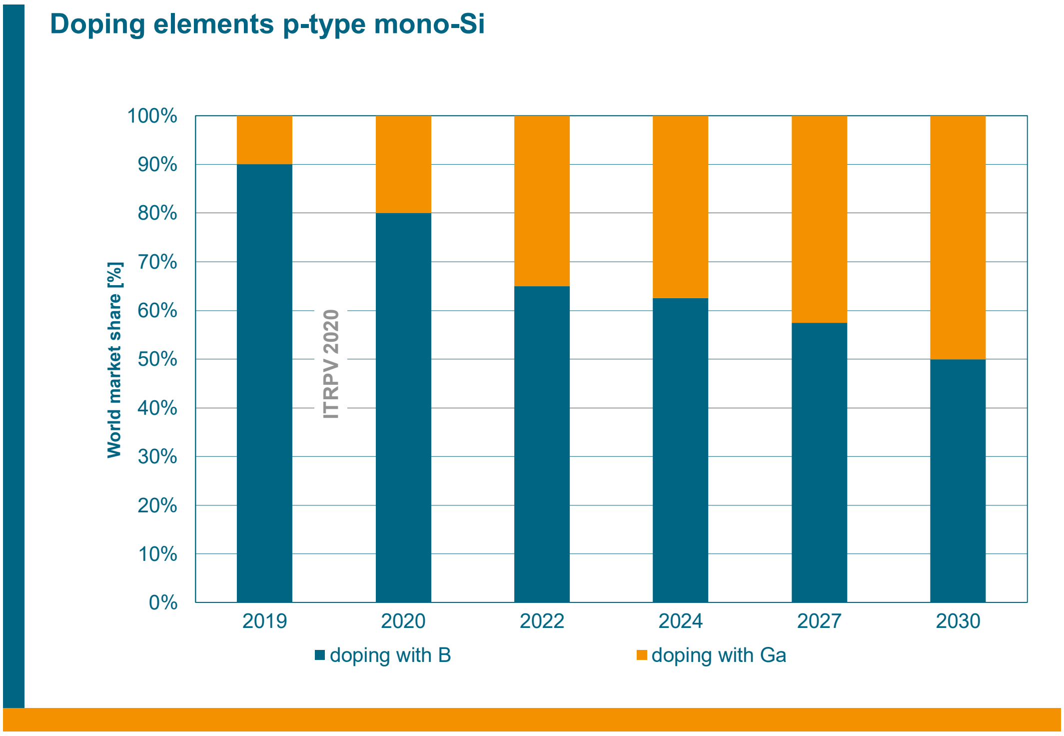


Fig. 8: Expected market share of elements used for doping of p-type mono-Si material.

Fig. 8 shows the expected market share of doping materials for p-type mono-Si. We expect an increasing share of Ga instead of B. Light induced degradation (LID) of p-type material is significantly reduced with gallium doping [17].

5.2.2. Wafering

The landscape in wafering technology changed completely during the last years. The introduction of diamond wire sawing (DWS), completed in 2018 for mono-Si and mc-Si wafering, was a significant improvement in terms of wafering process stability and cost reduction. DWS enables significant reductions of the kerf width and contributed therefore to the improved usage of poly-Si, as discussed in chapter 5.1. This transition was supported by the fast improvement of appropriate wet chemical processes for saw damage removal and texturing. Kerfless wafering technologies are not expected to contribute significantly to the future PV wafer market due to the maturity of DWS.

Fig. 9 describes the trend for kerf loss and for Total Thickness Variation (TTV). A kerf width of about 75 µm is standard today in diamond wire sawing (DWS). The kerf loss is predicted to decline to 50 µm within the next 10 years. Today's TTV of 20 µm is expected to be further improved to 10 µm until 2030.

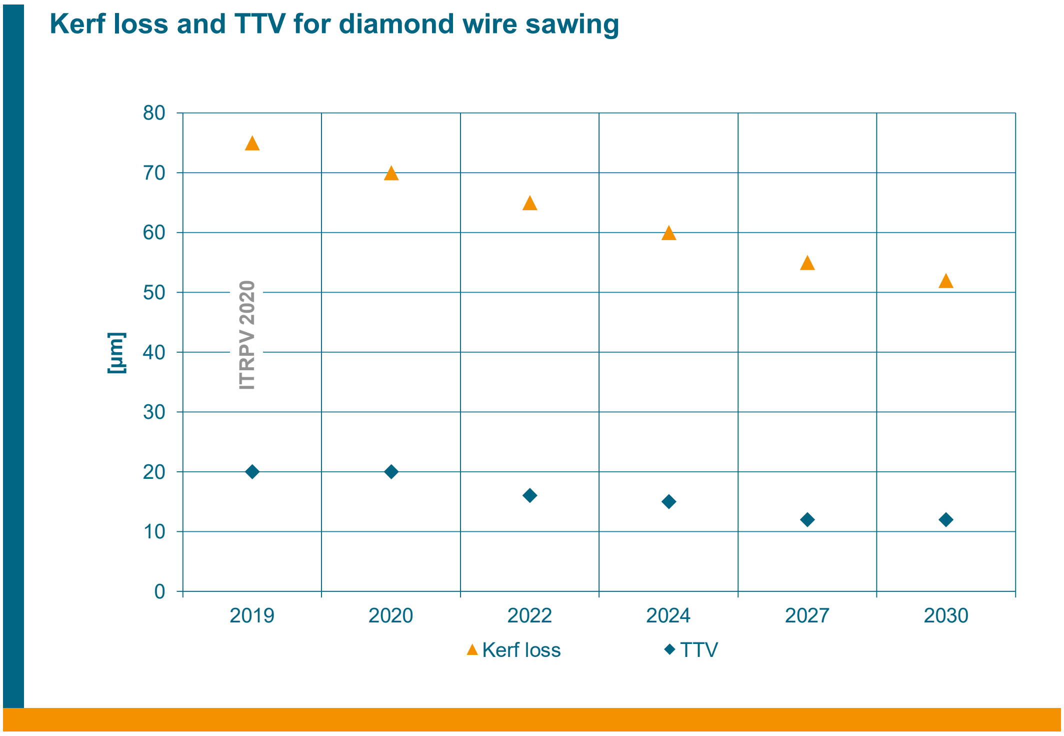


Fig. 9: Kerf loss and Total Thickness Variation (TTV) trend for diamond wire sawing.

5.2.3. Process Improvement Trends

Fig. 10: Throuput trend in crystal growth and wafer sawing.

Thinner wafers, reducing kerf loss, increasing recycling rates, and reducing the cost of consumables, will yield in cost savings. Wire diameters will be reduced continuously and there will be more recycling of silicon and diamond wire over the next years. Increased tool throughput will improve the productivity in crystallization and wafering on top of the yield enhancements by reduced kerf loss. This contributes to further cost optimization. Fig. 10 and Fig. 11 show the expected trends for throughput and conversion cost for crystallization and wafering. All technologies are expected to realize about 30% cost reduction during the next 10 years.

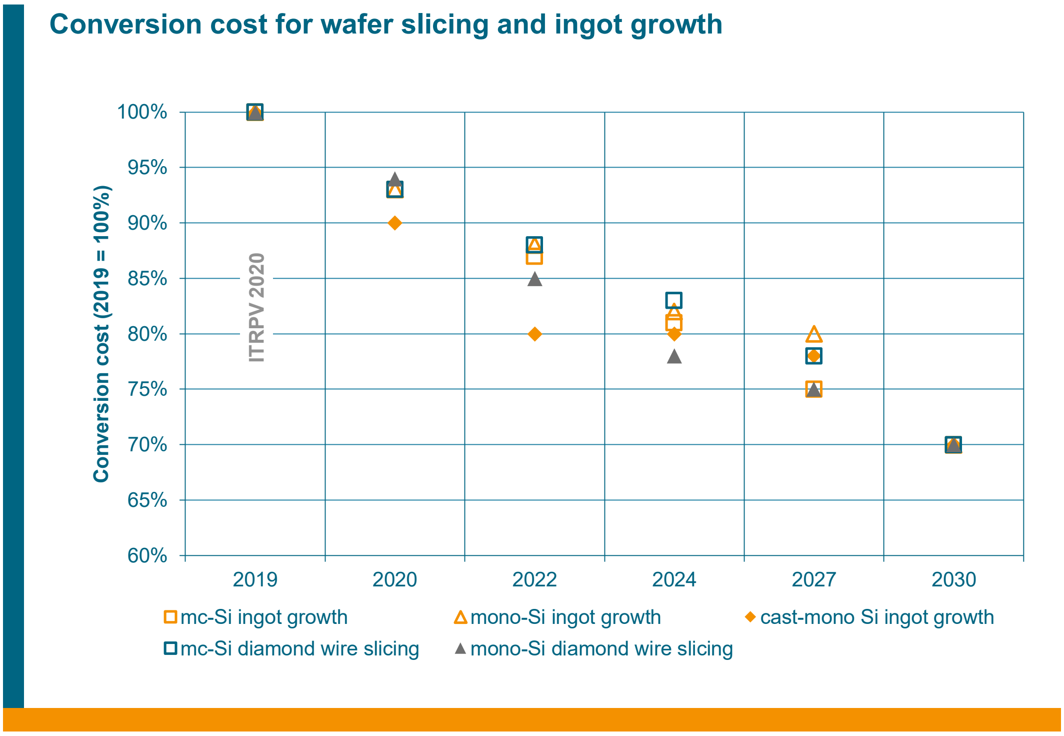


Fig. 11: Trend of conversion cost for crystallization and wafering technologies.

5.3.Products

Si wafers account for 51% of today's mc-Si cell price and for about 66% of mono-Si cells, as shown in Fig. 2 and Fig. 3. Reducing the as-cut wafer thickness will lead to more efficient use of silicon and cost savings.

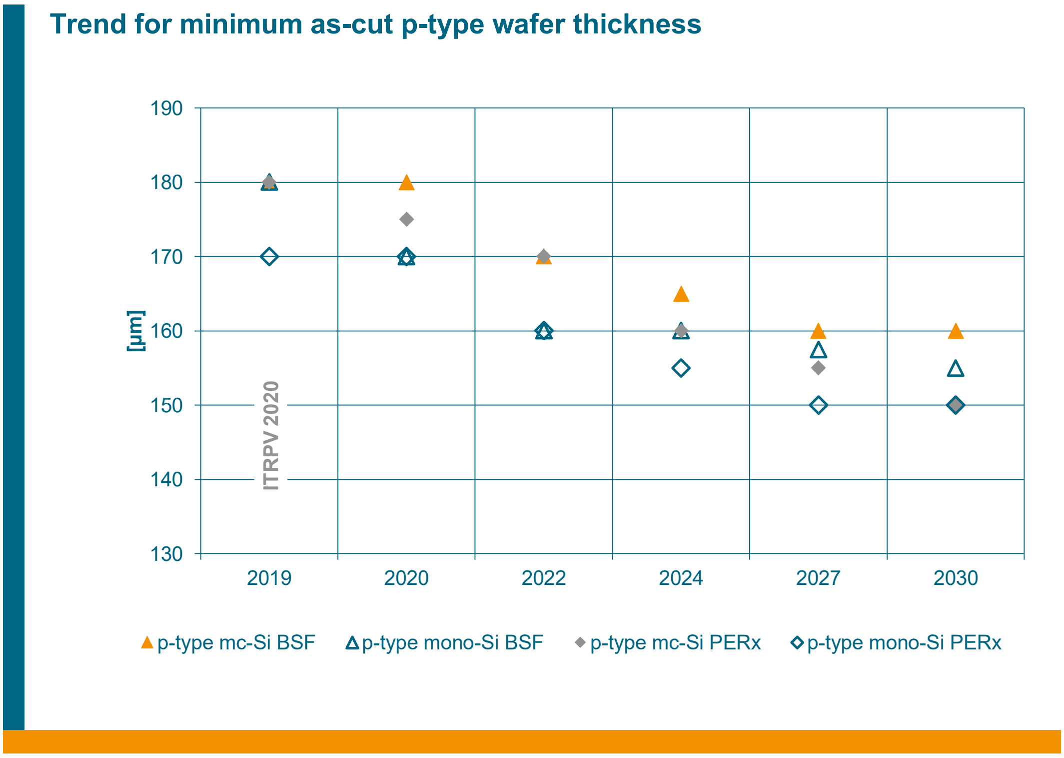


Fig. 12: Predicted trend for minimum as-cut wafer thickness p-type c-Si solar cell concepts.

The developments anticipated in previous editions of the roadmap did not materialize in the past, but we currently see that mono-Si wafer thickness was reduced: 170 µm are standard today for p-type mono PERC cells. But ≥ 175 µm thickness is still preferred for mc-Si as shown in Fig. 12. It is assumed that the thickness of mc-Si PERC wafers will slowly approach a minimum value between 160 and 150 µm until 2027. Mono-Si wafer thickness for PERC will reach 150 µm in 2027. The corresponding cell thickness limit trend in module technology is discussed in chapter 7.

Fig. 13 shows the predicted trend of as-cut wafer thickness for n-type mono-Si wafers. Current wafer thickness of HJT and IBC cells concepts is 160 µm with an expected fast reduction trend to 120 µm. N-type PERx cells follow a similar trend as p-type cells but with an expected minimum thickness of 140 µm in 2027.

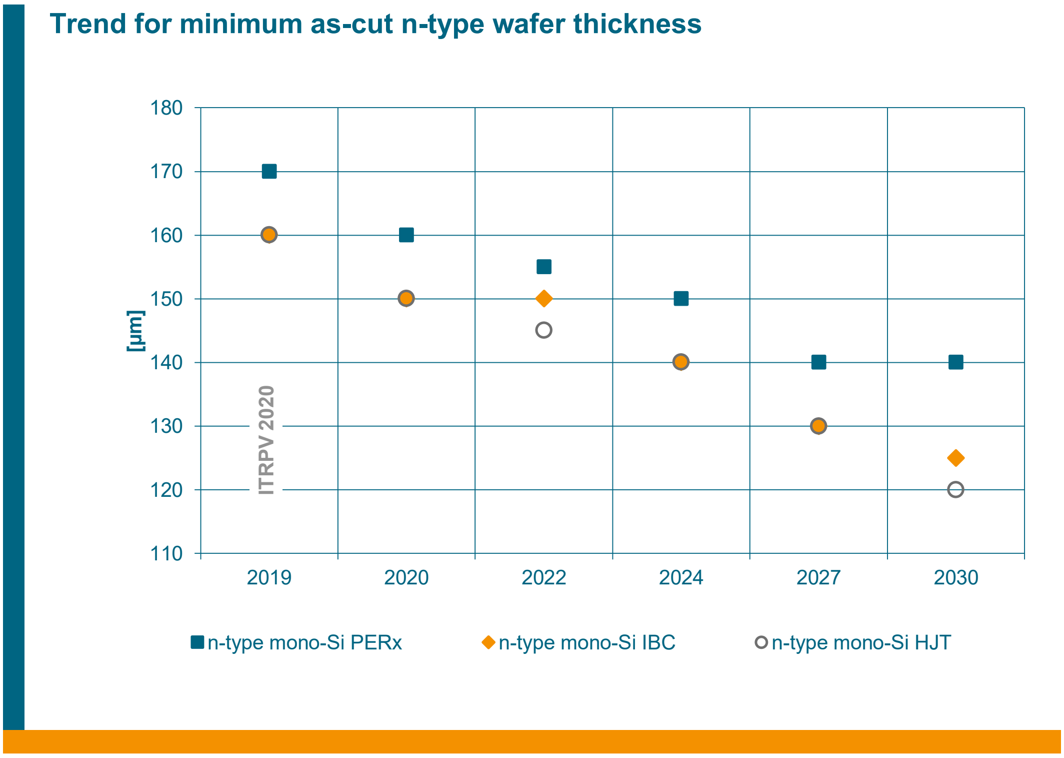


Fig. 13: Predicted trend for minimum as-cut wafer thickness n-type c-Si solar cell concept.

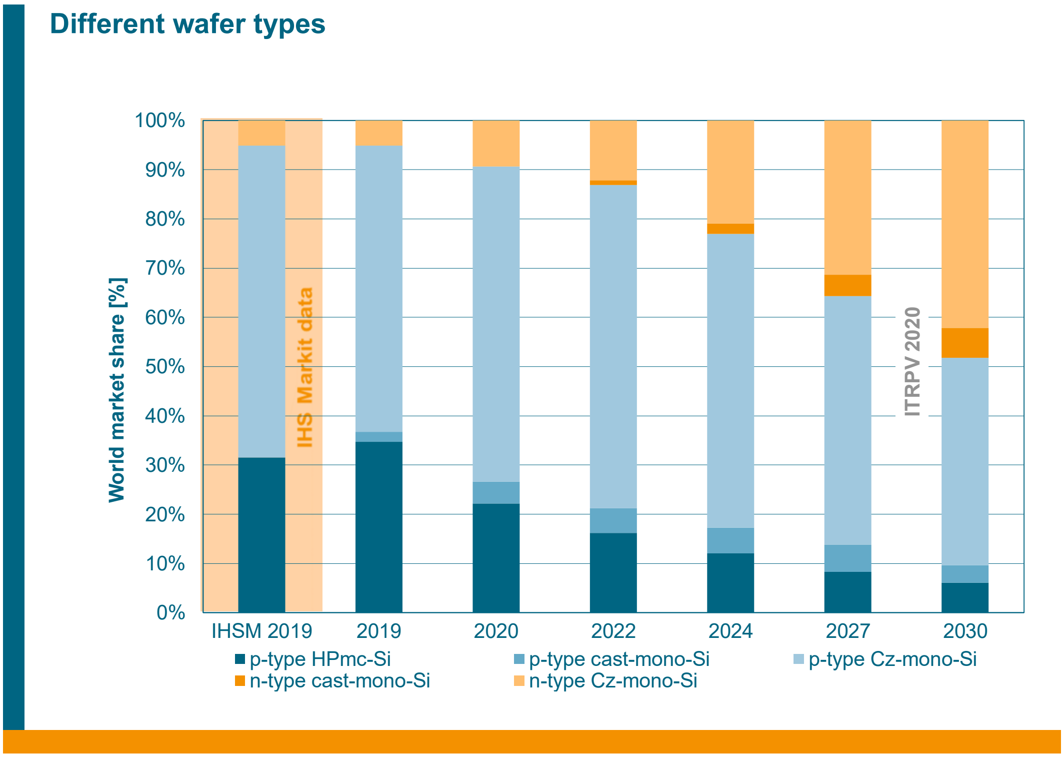


Fig. 14: Market share for different wafer types. IHS Markit data are indicated for 2019 as reference, [19].

Fig. 14 shows the expected market trend for different wafer types. Cz-mono-Si is clearly dominating the market. In 2019, Cz-mono-Si materials had a market share of about 65% vs. about 35% for cast-mono-Si materials and it is expected to gain further market share over casted materials of up to 80% in 2030. The trend of increased Cz-mono-Si market share is in line with the assumptions of previous ITRPV editions. Previous year market share predictions for Cz-mono-Si were surpassed as the trend was realized much faster than anticipated [18]. The plotted prediction of IHS Markit for 2019 shows that the ITRPV result is close to it [19]. The mono-Si market splits into n- and p-type. Casted materials are p-type doped high-performance mc-Si (HPmc-Si) and cast-mono-Si with p- and n-type doping respectively. The market share of cast-mono-Si materials will shrink continuously to below 10% in 2030. N-type mono-Si material is expected to gain > 40% in 2030. N-type cast-mono-Si is expected to appear in the market around 2022.

In the 11th edition of the ITRPV with included maturity report [20] we summarized the implementation possibilities of different wafer formats for mc-Si and for Cz-mono-Si as shown in Tab. 1. Wafer dimemsions of ≥ 166 x 166 mm² (M6) are only possible with new cell manufacturing capacities. So existing cell manufacturing capcities may only use formats < M6 without upgrades.

Tab. 1: Implementation status of new wafer formats.

Implementation of new Wafer Size in Production

Wafer manufacturing mc-Si	158.75 (+/-0,25) mm²	in existing lines possible
	161.7 (+/-0,25) mm²	possible with upgrades
	≥ 166 (+/-0,25) mm²	possible with new lines
Wafer manufacturing mono-Si	158.75 (+/-0,25) mm² (full- & semisquare)	in existing lines possible
	161.7 (+/-0,25) mm² (full- & semisquare)	possible with upgrades
	166 (+/-0,25) mm² (semisquare)	possible with upgrades
	≥ 166 (+/-0,25) mm²	possible with new lines
Cell manufacturing	158.75 (+/-0,25) mm² (incl. semisquare)	in existing lines possible
	161.7 (+/-0,25) mm² (incl. semisquare)	possible with upgrades
	166 (+/-0,25) mm² (incl. semisquare)	possible with new lines
	> 166 (+/-0,25) mm²	possible with new lines
Module manufacturing	158.75 (+/-0,25) mm²	in existing lines possible
	161.7 (+/-0,25) mm²	possible with upgrades
	≥ 166 (+/-0,25) mm²	possible with new lines

Fig. 15 and Fig. 16 show the ITRPV survey results about the market share of different wafer dimensions for cast-mono-Si wafers and for Cz-mono-Si, respectively. The move from the 6" format 156 x 156 mm² to the larger formats started in 2015. Today, 6" wafers disappeared completely.

We see a diversification in mc-Si wafer formats, powered by the growing market share of Cz-mono-Si. The 2019 dominating format of 156.75 x 156.75 mm² will disappear within the next 5 years and will be fast replaced by larger formats. Future mainstream after 2025 will be formats of 166 x 166 mm² (M6) and larger like 210 x 210 mm² (M12) with a share of ≈70% as shown in Fig. 15.

Fig. 16 shows that, also for Cz-mono-Si wafers the format of 156.75 x 156.75 mm² (M2) will disappear but even faster within the next 3 years. M2 has about 30% share in 2020. Larger formats as 158.75 x 158.75 mm² (G1), 161.75 x 161.75 mm² (M4), 166 x 166 mm² (M6), and 210 x 210 mm² (M12) have in 2020 about 70% market share - 35% G1, 20% M4, and 15% M6. M12 is currently introduced in the market [21].

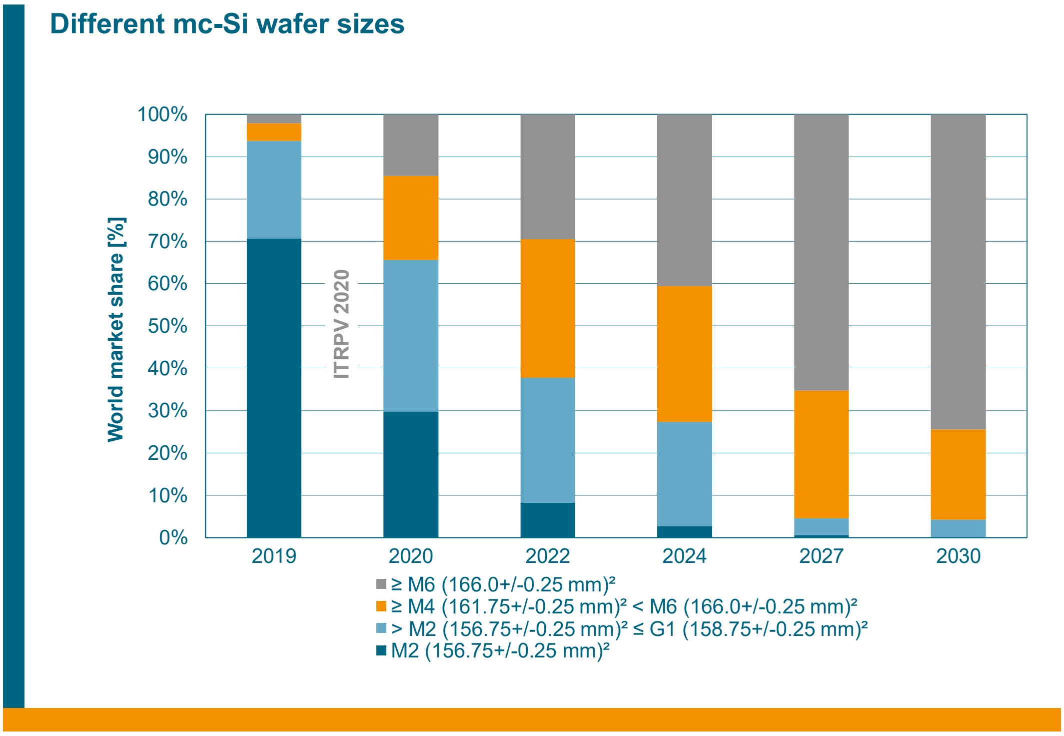


Fig. 15: Expected trend of mc-Si wafer size in mass production.

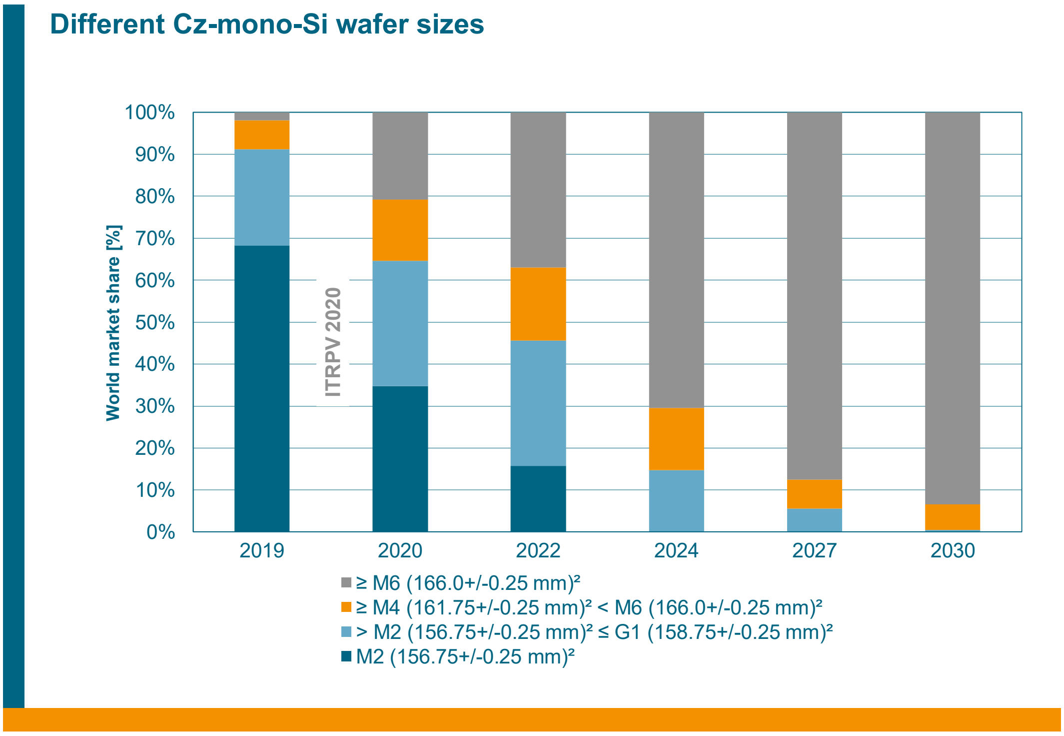


Fig. 16: Expected trend of Cz-mono-Si wafer size in mass production.

We assume that M4 will keep a future market share between 10% and 20% during the next 5 years. M6 and larger formats will gain significant market share in mono-Si within the next years in parallel with new cell capacity expansions. Market penetration of M12 format will depend on the acceptance of the corresponding new module products [22].

The dimension change for Cz-mono-Si goes along with an increase in diameter of the pseudosquare wafers: 223 mm will fast gain market share as shown in Fig. 18. This diameter is characteristic for G1 and M4. With the new formats and diameters, fullsquare wafers are becoming more interesting - 223 mm diagonal is present in 158.75 x 158.75 mm² FSQ wafers, Fig. 17 shows the estimated trend.

A standardization of the different wafer formats is necessary to enable availability of appropriate production machines and materials like glass and foils especially for the manufacturing of modules with new wafer formats. SEMI is currently working to update the Si wafer spec for PV solar cells [23].

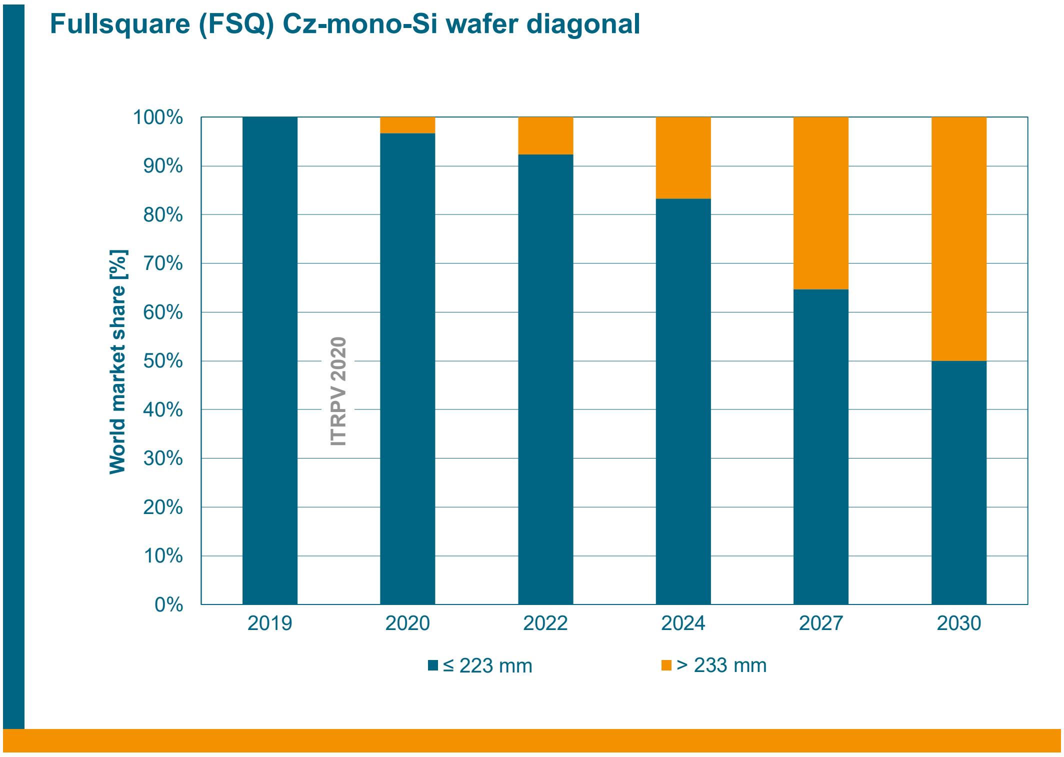


Fig. 17: Trend of wafer diogonal for full-square (FSQ) Cz-mono-Si wafers.

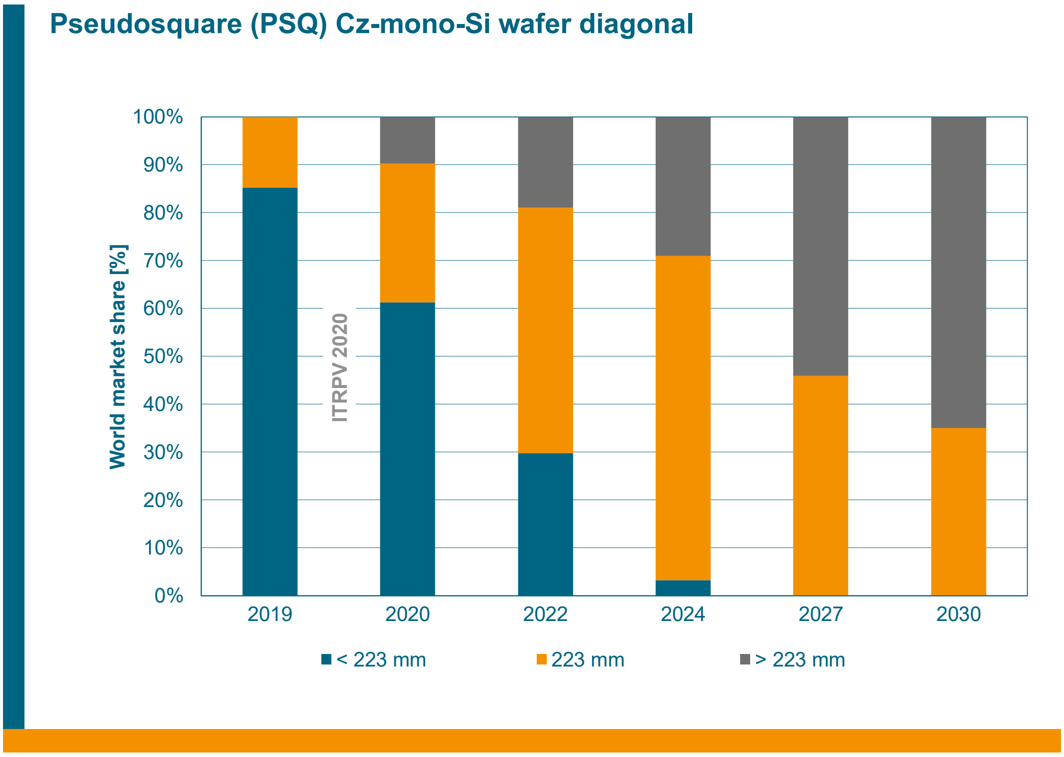


Fig. 18: Trend of wafer diagonal for pseudosquare (PSQ) Cz-mono-Si wafers.

Wafer manufacturing will be done in larger fabs with annual production capacities well above 2 GW as shown in Fig. 19.

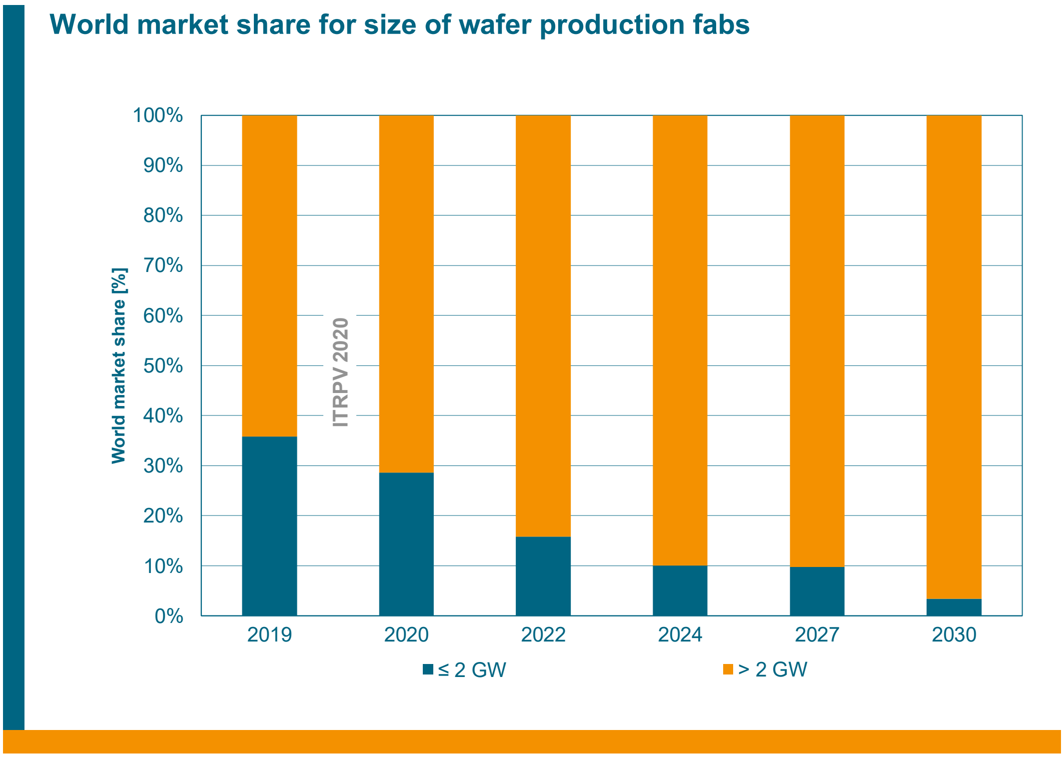


Fig. 19: Trend of annual capacity of wafer production fabs.

6. Result of 2019 | Cell

6.1.Materials

Metallization pastes/inks containing silver (Ag) and aluminum (Al) are the most process-critical and most expensive non-silicon materials used in current c-Si cell technologies. Paste consumption therefore needs to be reduced.

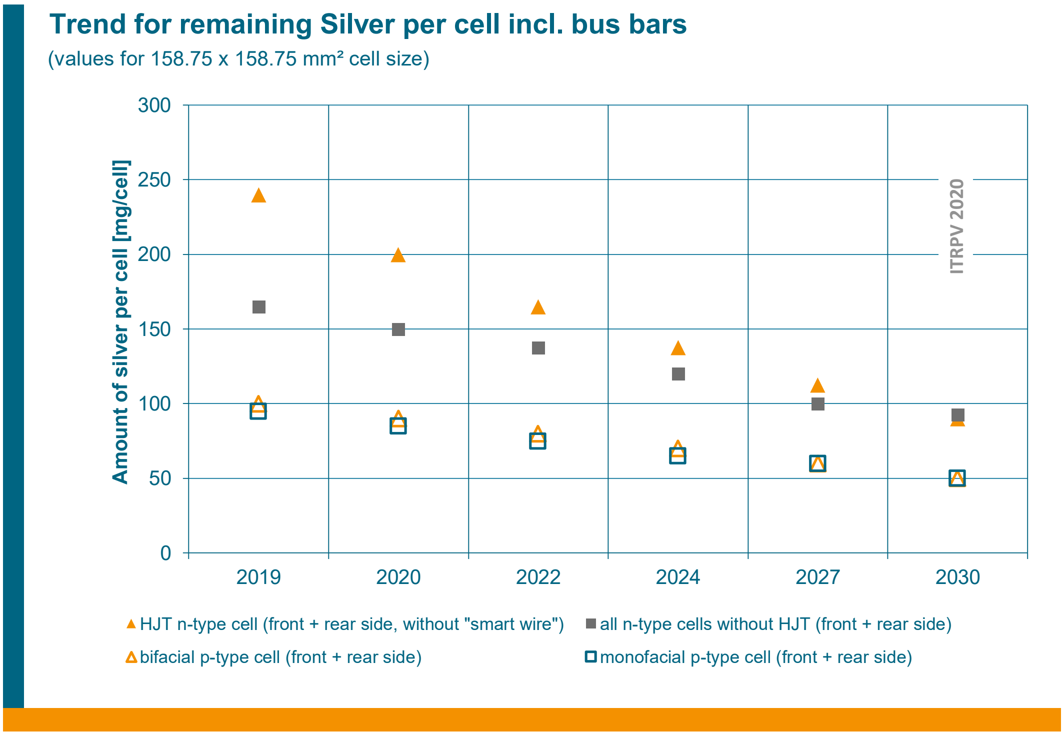


Fig. 20: Trend for remaining silver per cell for different cell concepts (158.75 x 158.75 mm²).

Fig. 20 shows our estimations regarding the future reduction of the silver that remains on 158.75 x 158.75 mm² cells of different p- and n-type cell concepts after processing. The 2.5% cell area increase compared to former editions of the ITRPV is quite low and does not influence the trend.

The reduction of remaining silver per cell is expected to continue during the next years. The current study found still 100 mg as the median value for 2019 and 90 mg for 2020 - revealing that there was no big progress in laydown reduction. Anyhow, a reduction down to 50 mg per cell is still expected to be possible within the next 10 years. New developments in pastes and screens must enable this reduction, and this clearly shows the necessity of a close collaboration between suppliers and cell manufacturers to meet these challenges. The average silver price of 560 US$/kg beginning of March 2020 [24] results in costs of 5 US$ cents/cell (0.91 US$ cents/Wp for a 22% mono PERC cell), or ≈25% of the non-wafer mono cell price, discussed in chapter 4. For a mc-Si cell with top efficiency of about 20.5% this corresponds to 1.03 US$ cent/Wp, also ≈25% of the non-wafer mc-Si price.

N-type cell concepts show a significant higher silver consumption than p-type cells as silver is used for front and entire rear side metallization. Bifacial p-type concepts cause no difference in silver consumption.

Because silver will remain expensive due to the world market dependency, it is extremely important to continue all efforts to lower silver consumption as a means of achieving further cost reductions. Despite a continuous reduction of silver consumption at the cell manufacturing level, silver replacement is still considered. Copper (Cu), as less expensive material, applied with plating technologies, is the envisioned substitute, today in use only for high efficiency back contact cell concepts. It is still assumed that it will be introduced in mass production, but the market share is considered as conservative as in the last edition with about 15% in 2030 expectations. Technical issues related to reliability and adhesion must be resolved before alternative metallization techniques can be introduced. Appropriate equipment and processes also need to be made ready for mass production. Silver is expected to remain the most widely used front metallization material for c-Si cells in the years to come.

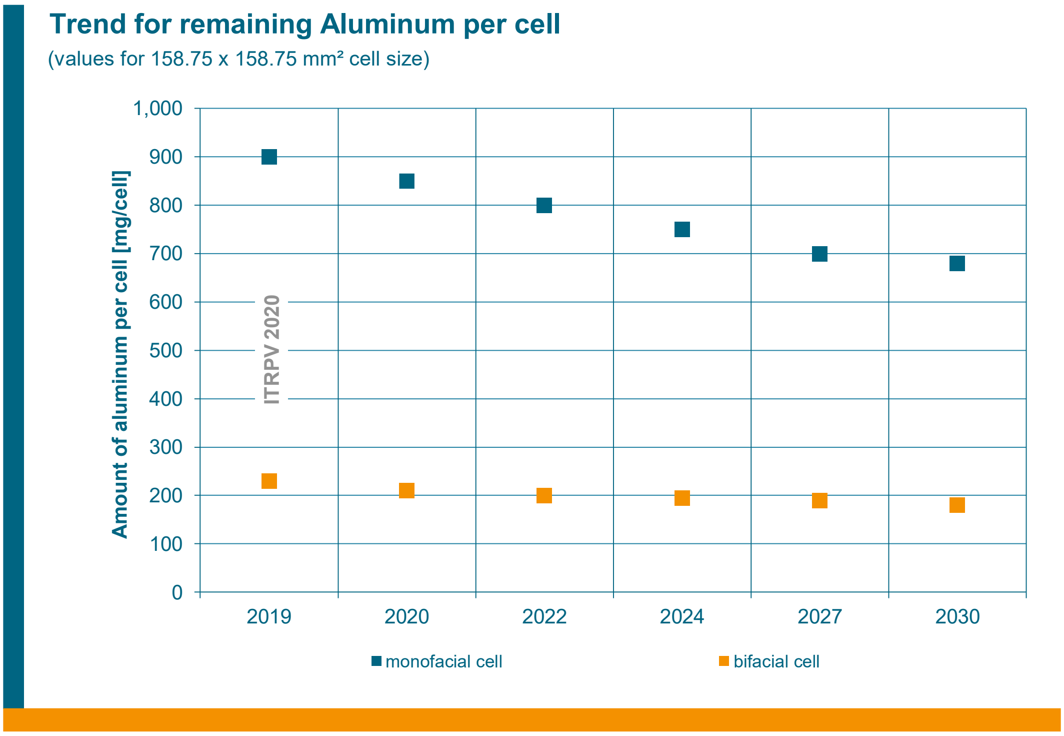


Fig. 21: Trend for remaining aluminum per cell for monofacial and bifacial PERC concepts (158.75 x 158.75 mm²).

The trend of remaining aluminum is shown in Fig. 21. We distinguish in this figure between bifacial and monofacial cell concepts using BSF or PERC technologies. Bifacial cells need much less aluminum - only about 25% of the corresponding monofacial cell type. The reduction is assumed to reach down to 680 mg for monofacial and 180 mg for bifacial cell concepts, respectively.

Materials containing lead are restricted in accordance with legislation that went into effect in 2011 under the EU Directive on the Restriction of Use of Hazardous Substances (RoHS 2). This restriction affects the use of lead and other substances in electric and electronic equipment (EEE) on the EU market. It also applies to components used in equipment that falls within the scope of the Directive. PV panels are excluded from RoHS 2, meaning that they may contain lead and do not have to comply with the maximum weight concentration thresholds set out in the directive[1]. PV's exclusion will surely remain in effect until a review of RoHS 2 will likely take place by mid-2021 at the latest[2].

[1] Article 2(i) of the RoHS Directive [2011/65/EU] excludes from the scope of the Directive "photovoltaic panels intended to be used in a system that is designed, assembled and installed by professionals for permanent use at a defined location to produce energy from solar light for public, commercial, industrial and residential applications."

[2] Article 24 of the RoHS Directive [2011/65/EU] requires an evaluation and possible revision of the Directive, including its scope, by July 22, 2021.

Cell and module manufacturers should act carefully, especially, as the exclusion in question is limited to PV panels installed in a defined location for permanent use (i.e. power plants, rooftops, building integration etc.). Should the component in question also be useable in other equipment that is not excluded from RoHS 2 (e.g. mobile charging applications), then the component must comply with the Directive’s provisions.

We anticipate lead free pastes to become widely used in the mass production of c-Si cells. Fig. 22 shows that during the next years the cells will become more and more lead free.

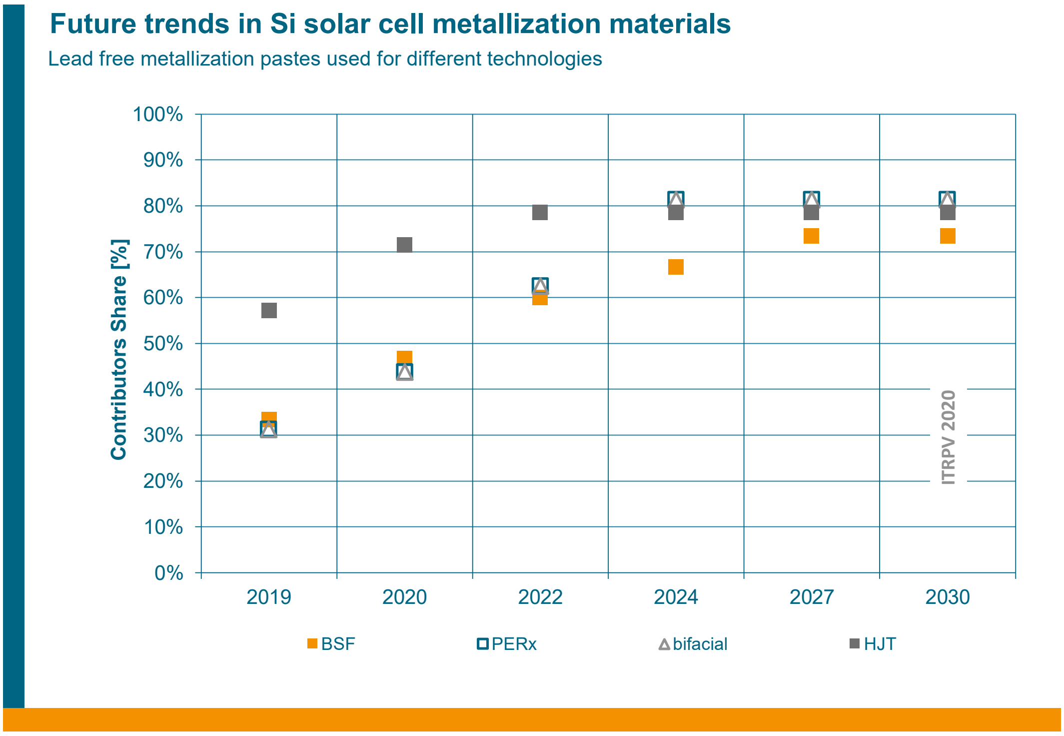


Fig. 22: Trend for implementation of lead free pastes in different cell technologies.

6.2.Processes

The first production process in cell manufacturing is texturing. Reducing the reflectivity is mandatory to optimize cell efficiency. The expected market share of different texturing methods for mc-Si is shown in Fig. 23. Acidic texturing, a wet chemical process, is mainstream in current mc-Si cell production. Wet chemical processing is a very efficient and cost optimized process especially due to its high throughput potential as discussed in Fig. 23. Standard acidic texturing including the use of additives is expected to stay mainstream until 2024. Especially the application of additives enabled good texturing of DWS mc-Si material. Progress in metal catalyzed chemical etching (MCCE) or wet chemical nano-texturing technologies is causing the expectation that MCCE will become dominant after 2024. Reactive ion etching (RIE) is not expected to reach > 2% market share due to the higher costs.

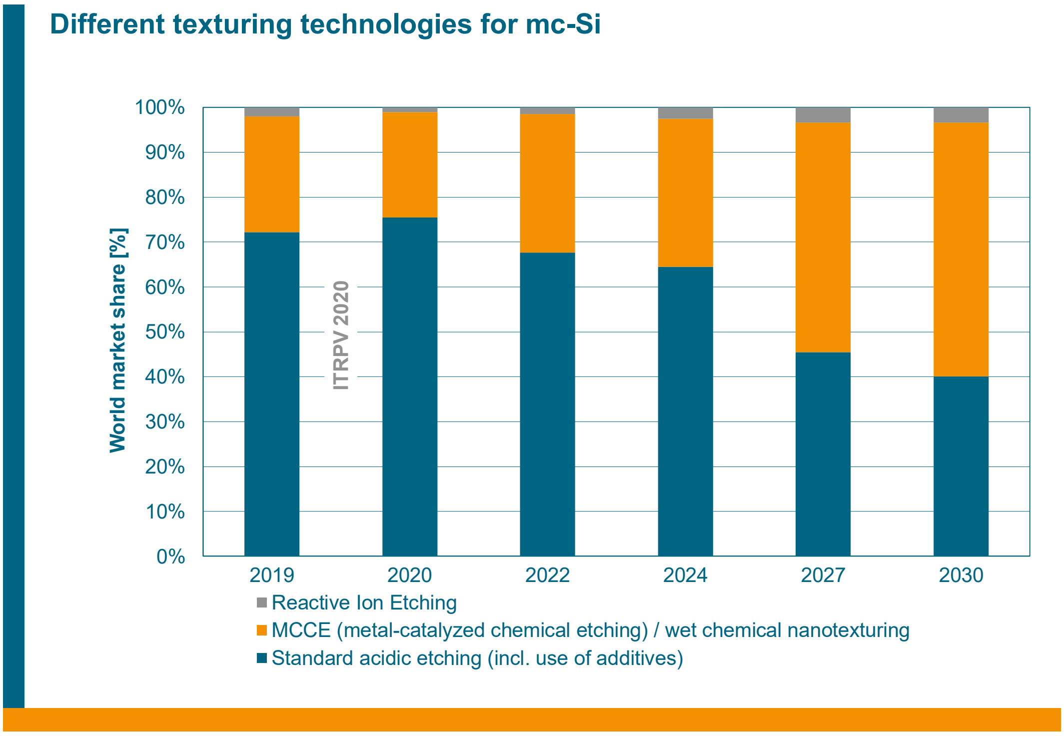


Fig. 23: Expected market share of different texturing methods for mc-Si.

Solar cell recombination losses on the front and rear sides of the cell, as well as recombination losses in the c-Si bulk material, must be reduced in line with high-efficiency cell concepts. The recombination currents J0bulk, J0front, J0rear, indicating the recombination losses in the volume, on the cell's front and rear side respectively, are a reasonable way to describe recombination losses. Fig. 24 and Fig. 25 show the expected recombination current trends for p-type and n-type materials, respectively.

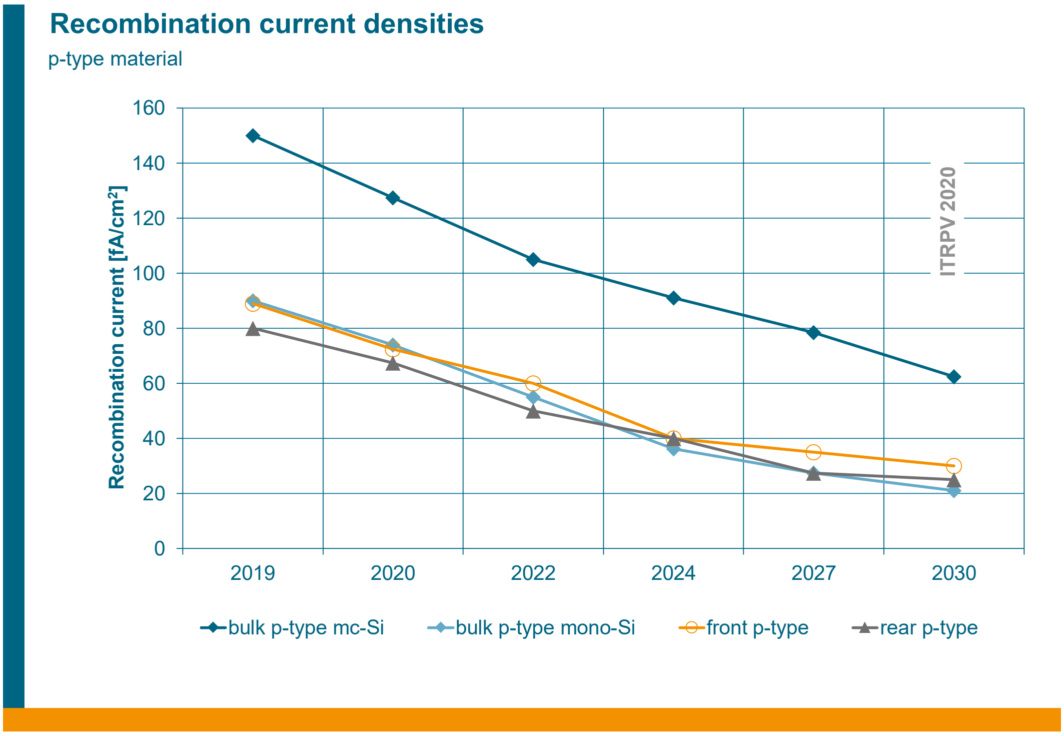


Fig. 24: Predicted trend for recombination currents J0bulk, J0front, J0rear for p-type cell concepts.

The values are in line with the assumptions of former ITRPV editions. Recombination currents can be measured as described in literature [25], or they can be extracted from the IV curve if the other J0 components are known. As shown in Fig. 24 the improvement of the silicon material quality for both, mono-Si and mc-Si will continue. This should result in a reduction of the J0bulk value to 60 fA/cm² for p-type mc-Si and about 20 fA/cm² for p-type mono-Si. J0front and J0rear are expected to improve similar like p-type mono-Si to below 30 fA/cm² in 2030. Reductions of J0bulk will result from further improvements of the crystallization process (see chapter 5.2.). The introduction of improved casting processes (e.g. HPmc-Si) resulted in lower bulk recombination currents for mc-Si material. J0 values of front and rear surfaces are similar for different bulk materials. This J0 values are expected to be reduced by up to 70% of the current values by 2030.

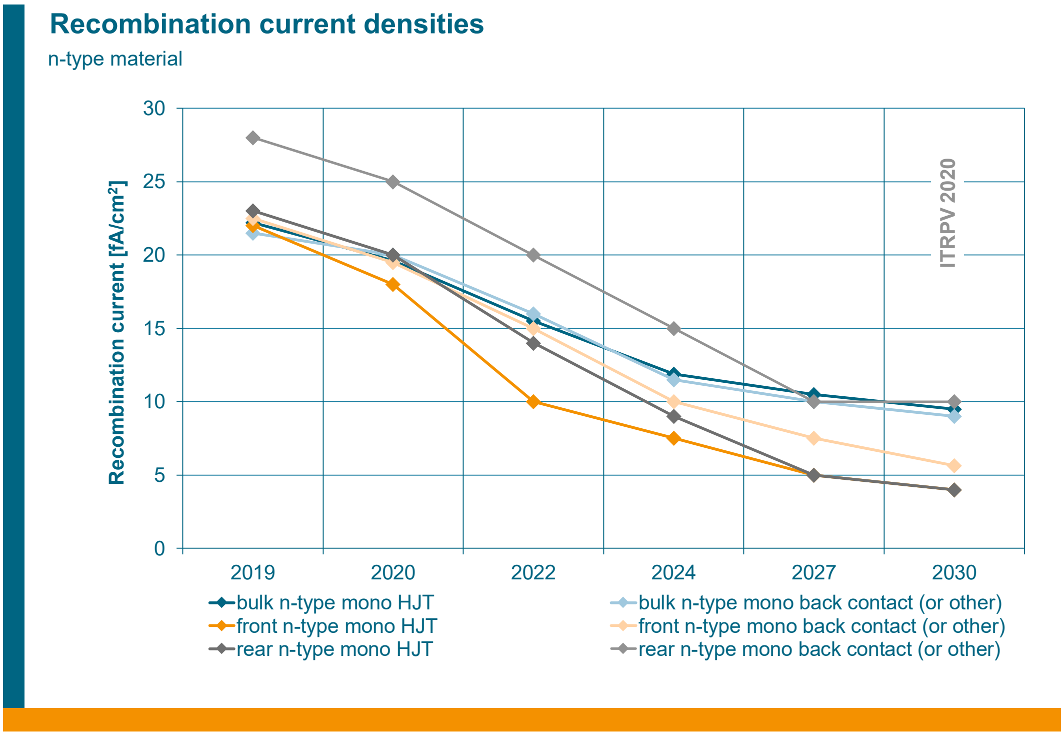


Fig. 25: Predicted trend for recombination currents J0bulk, J0front, J0rear for n-type cell concepts.

Fig. 25 shows that today's n-type mono-Si wafers have J0bulk value of < 30 fA/cm², about 30% of the corresponding p-type J0bulk value. J0front and J0rear are also lower for n-type concepts emphasizing the potential for higher cell efficiencies. It is expected that all values will be further reduced to about 10 fA/cm² within the next 10 years. J0rear improvements are linked closely to cell concepts with passivated rear side.

Since 2012, several cell concepts using rear side passivation with dielectric layer stacks have been in mass production (PERC/PERT/PERL technology). Fig. 26 shows the expected market shares of different rear side passivation technologies suitable for n-type and p-type PERx cell concepts. Remote plasma PECVD Al_2O_3 in combination with a capping layer has a market share of 55% in 2020 - this former mainstream technology for PERC cell concepts will further lose market share. Newly built cell production capacities will use ALD Al_2O_3 deposition in combination with separate capping layer deposition, and direct plasma PECVD Al_2O_3 with integrated capping layer deposition. Tools combining ALD Al_2O_3 and PECVD SiN_x will also be available in the market. PECVD $SiON_x/SiN_x$ is considered as niche process.

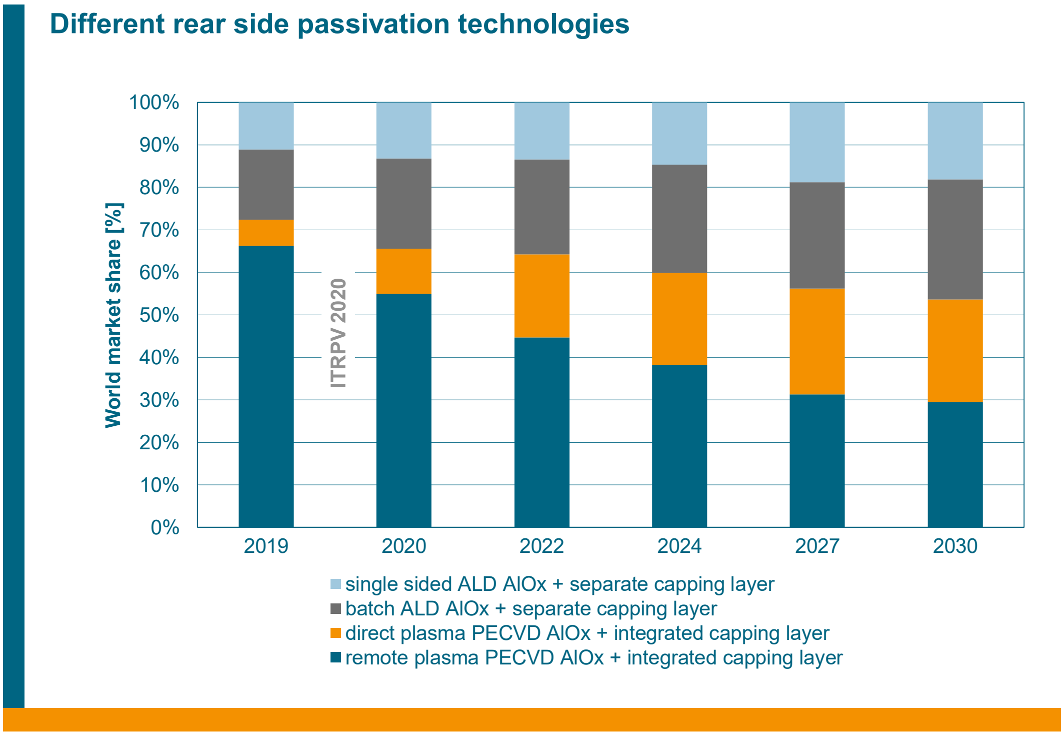


Fig. 26: Predicted market shares for AlO_x-based rear side passivation technologies.

A new method for rear side passivation uses a thin tunneling oxide layer with a conducting polysilicon cap layer. Instead of forming contacts to the bulk silicon the contacting is done via tunneling of electrons. This technique avoids the forming of undesired recombination centers.

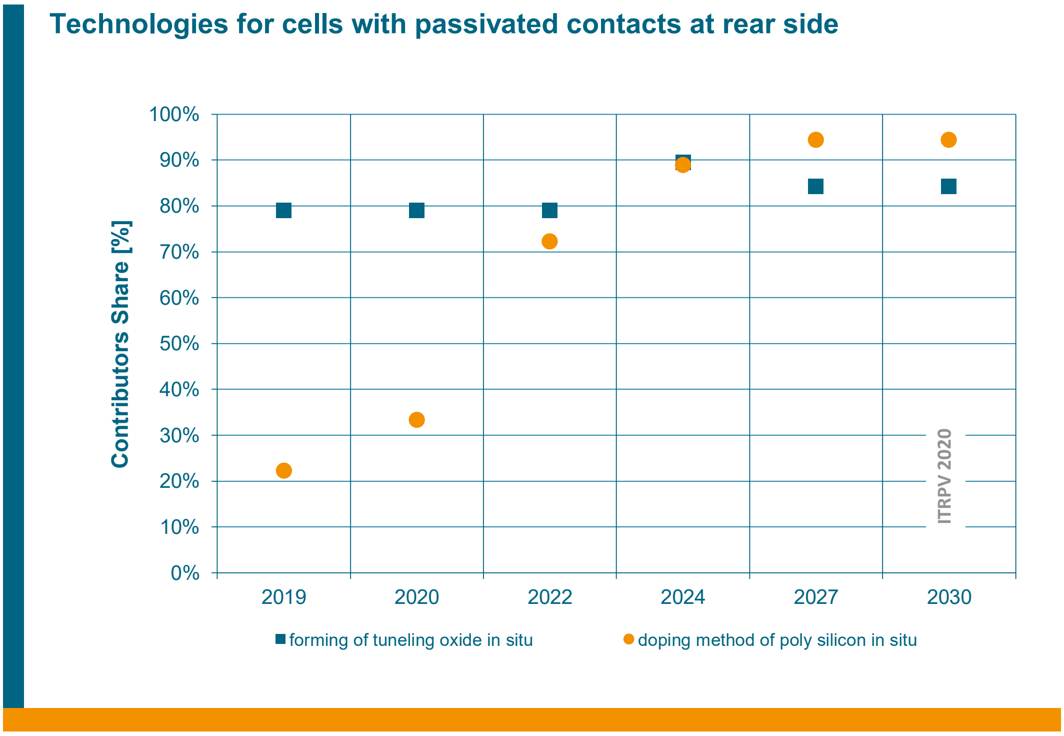


Fig. 27: Expected trend for forming the tunnel oxide and doping the ploy Si capping layer in passivated contact forming.

Fig. 27 shows the expected trend for the forming of the tunnel oxide and the method of doping the conducting poly-Si layer. In situ processing is expected to become the preferred technique. Market shares of this new technology will be discussed in chapter 6.3. The forming of the poly-Si layer can be done by LPCVD or by PECVD. There is no clear trend visible about which technology will become industry standard.

J0front improvements concern all relevant front side parameters (emitter, surface, contacts). A parameter that influences recombination losses on the front surface is the emitter sheet resistance. High sheet resistances are beneficial for low J0front - sheet resistances above 100 Ohm/square can be realized with and without selective emitters. If a selective emitter is used, sheet resistance values refer only to the lower doped region.

Fig. 28 shows the current situation for homogenous and selective Phosphorus doping: today's sheet resistance of homogenous doped p-type emitters is > 110 Ohm/square and it is expected to increase to 140 Ohm / square. Selective doping allows higher sheet resistances: the 130 Ohm/square in 2019 are expected to increase beyond 180 Ohm/square within the next years.

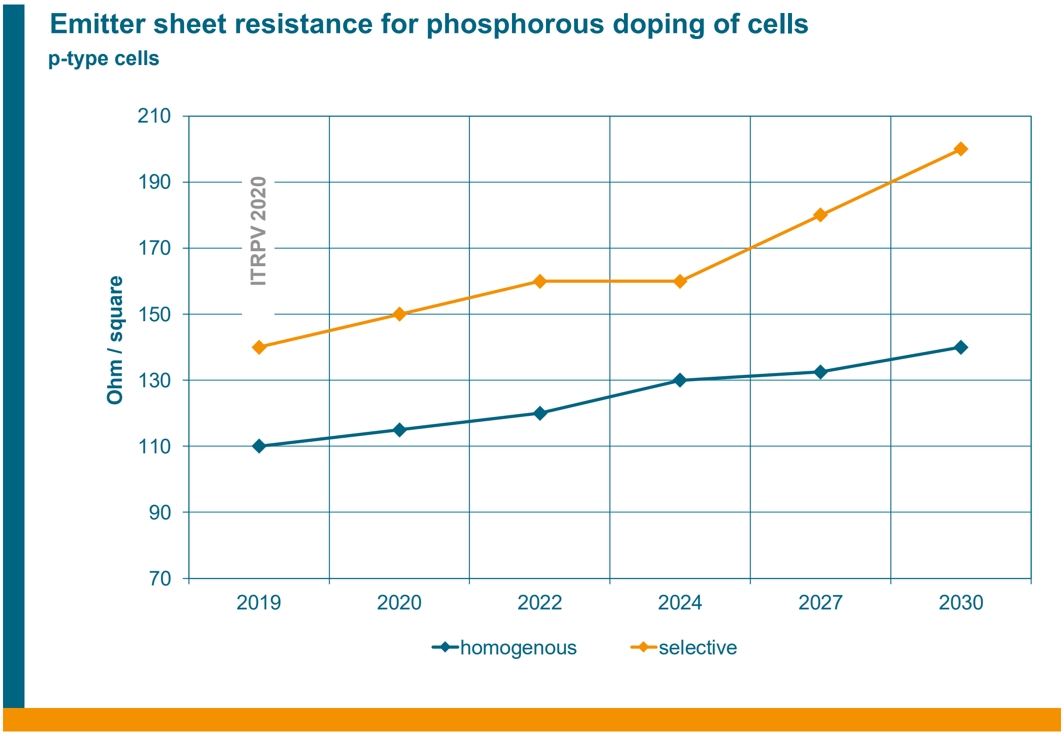


Fig. 28: Expected trend for emitter sheet resistance of Phospore doped emitters for p-type cell concepts. In case of selective emitter the sheet resistance value refers only to the lower doped region.

The predicted trend for n-type emitters is shown in Fig. 29. An emitter sheet resistance of about 100 Ohm/square is mostly used in today's boron diffused emitters. An increase to 120 Ohm/square is expected within the next years.

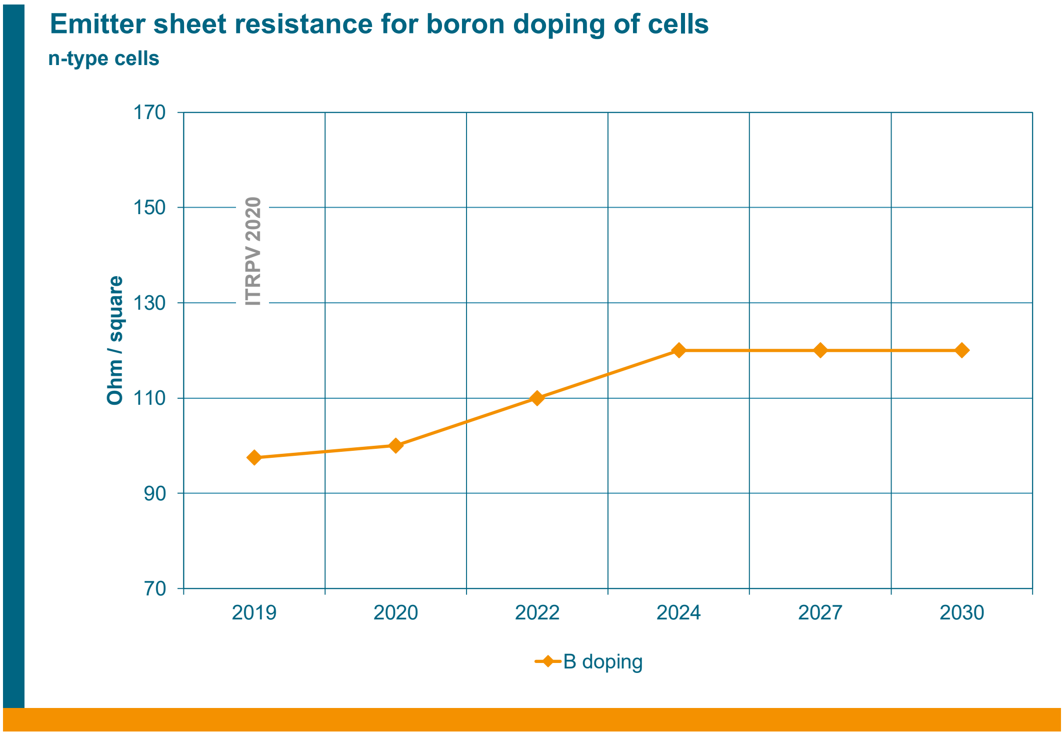


Fig. 29: Expected trend for emitter sheet resistance for boron doping for n-type cell concepts.

Fig. 30 shows the expected market share of different technologies for phosphorous doping in p-type cell processing. Homogeneous gas phase diffusion is a mature, cost efficient doping technology and will remain the mainstream for the years to come. Nevertheless, we see that - on top of gas phase diffusion - selective emitter processes are commonly used in mass production with shares of > 30% in 2019. The share of laser doped selective emitters will increase and become mainstream after 2024. Etch back selective emitter techniques or ion implantation will disappear soon.

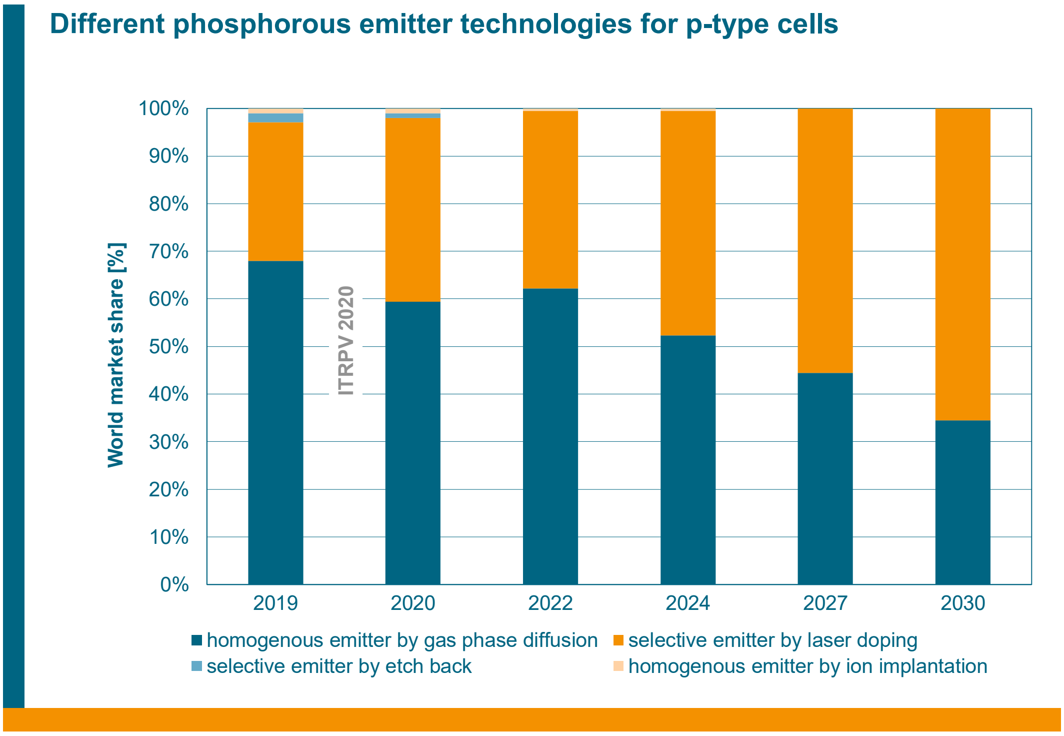


Fig. 30: Expected market share for different phosphorous emitter technologies for p-type cells.

Boron doping technologies for n-type cells, as shown in Fig. 31 will mainly use BBr_3 thermal diffusion technique. This is in line with the findings of the former ITRPV editions. Ion implantation is supposed to stay at low share of < 1% and BCl_3 doping is not expected to grow beyond 10% market share. Alternative processes are not seen with significant market shares so far.

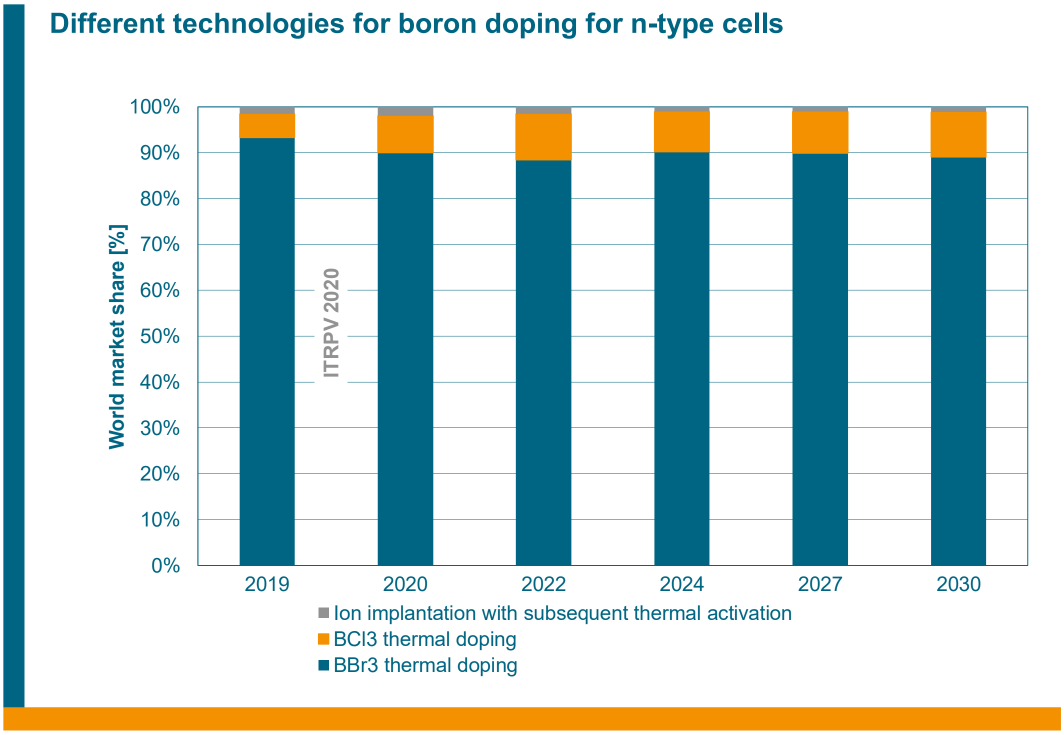


Fig. 31: Expected market share for different technologies for boron doping for n-type cells.

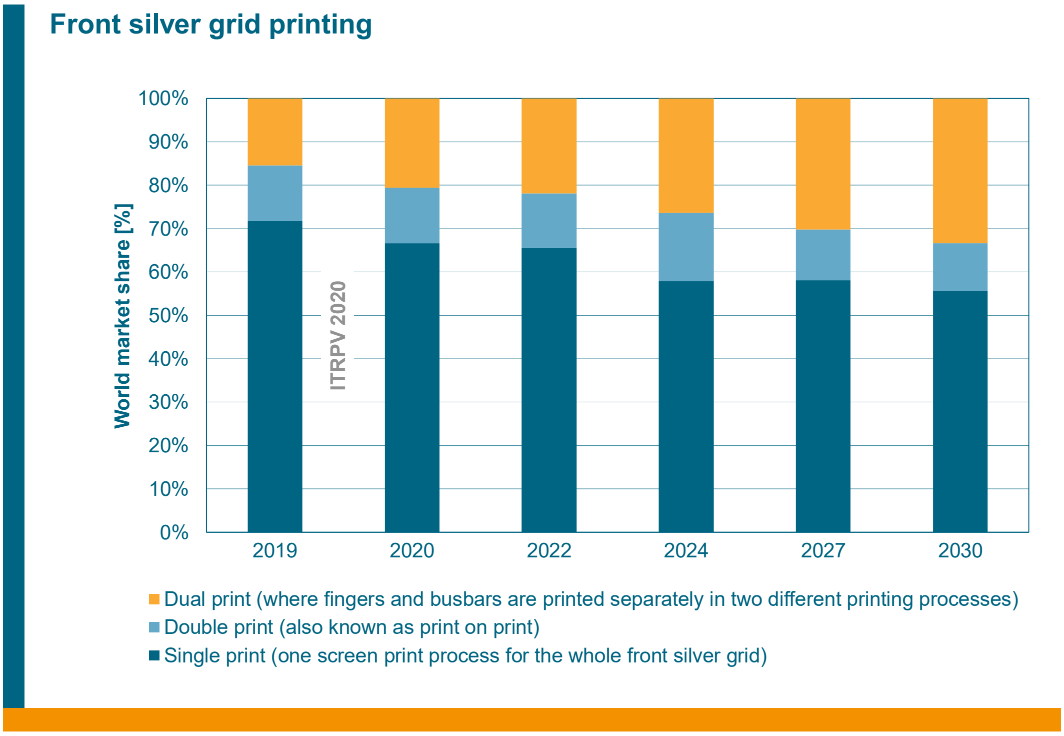


Fig. 32: Expected market share of different front side printing techniques.

Different approaches for high quality front side print exist. Fig. 32 summarizes the available technologies and their estimated market share during the next 10 years. Front metallization is a key process in the production of c-Si solar cells. New front side metallization pastes enable the contacting of the previously discussed low doped emitters without any significant reduction in printing process quality. Single print technology is mainstream, followed by dual printing. Double printing has a constant market share between 15% and > 10%. Dual und double print require an additional printing step with fine-alignment capabilities.

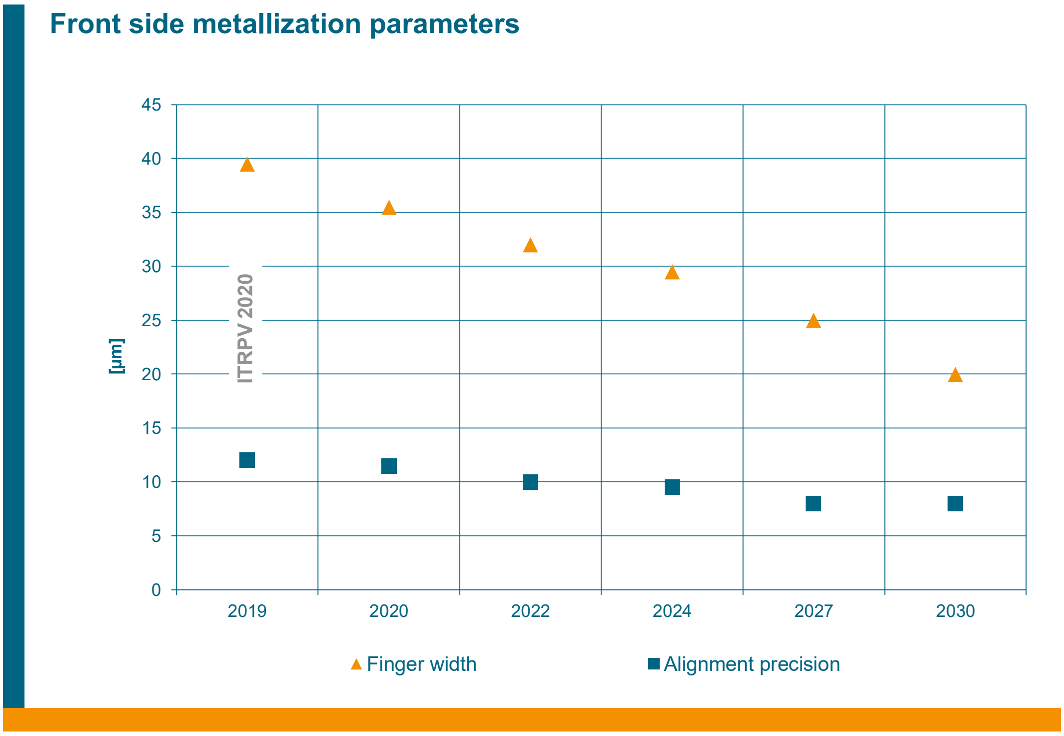


Fig. 33: Predicted trend for finger width and alignment precision in screen-printing. Finger width needs to be reduced without any significant reduction in conductivity.

Dual print separates the fingerprint from the busbar (BB) print, enabling the use of busbar pastes with less silver. Busbar less cell interconnect techniques can even omit the busbars completely. Therefore, for reliable module interconnection, and for applications as bifacial cells, a good alignment accuracy is important in metallization - an alignment accuracy of about 10 µm (@+/- 3 sigma) will be required from 2022 onwards as shown in Fig. 33. A reduction in finger width is one method yielding in efficiency gain and cost reduction, but only if it is realized without significantly increasing finger resistance. Furthermore, contact with a shallow emitter needs to be established reliably. One possible way to achieve these goals is to use a selective emitter structure, preferably without increasing processing costs. Reducing finger width reduces shadowing, but a trade-off has to be made to maintain conductivity if the roadmap for silver reduction as discussed in chapter 6.1. will be executed. Finger widths < 40 µm were standard in 2019. A further reduction to 20 µm appears possible over the next 10 years.

As mentioned above, reducing the finger width requires a tradeoff - a current trend in metallization that is direct related to the number of busbars used in the cell layout. Fig. 34 shows the expected trend. We see that the 3 and 4-BB layouts are disappearing and will be fast replaced by layouts with 5 and 6 or more BBs - and by BB-less layouts. BB-less technologies support minimum finger widths as shown in the Fig. 33 trend. Nevertheless, this will require new interconnection technologies in module manufacturing that - in best case - should be implemented by upgrading of existing stringing tools.

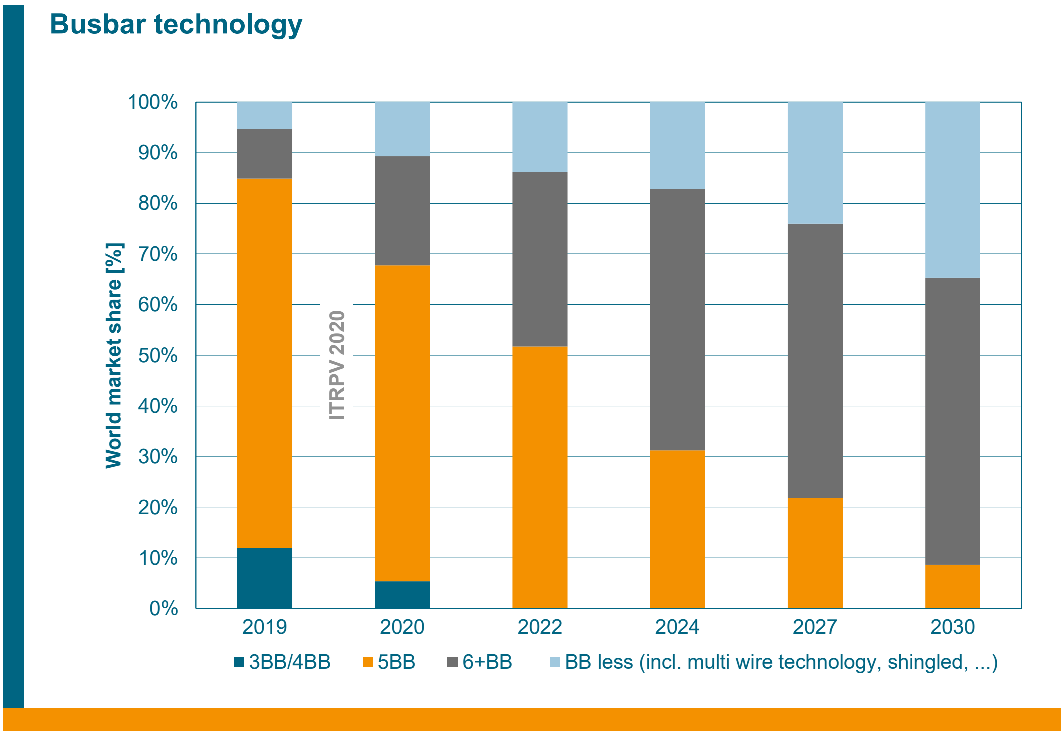


Fig. 34: Worldwide market share for different busbar technologies.

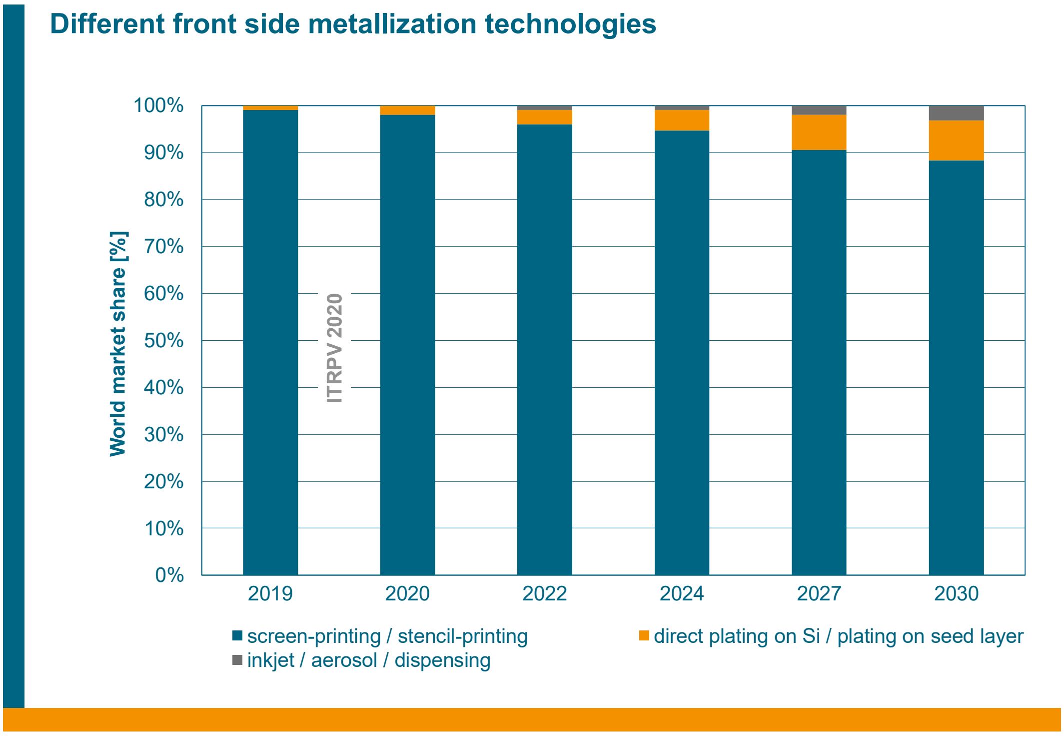


Fig. 35: Predicted trend for different front side metallization technologies.

Which technology will be used for the metallization in future? The expected share of different technologies for front side and rear side metallization are shown in Fig. 35 and Fig. 36, respectively. Fig. 35 shows that classical screen-printing will remain the mainstream technology for the years to come in front side metallization.

Stencil-printing is considered as advancement of screen-printing using stencils as a further development of screens. Plating is still considered as front side metallization technology with market shares above 5% from 2024 onwards. Other technologies like aerosol, inkjet or dispensing techniques are niche applications.
Screen-printing as well is expected to stay mainstream in rear side metallization for the next years as Fig. 36 shows. Other technologies are not expected to gain significant market share. Physical vapor deposition (PVD) disappeared completely.

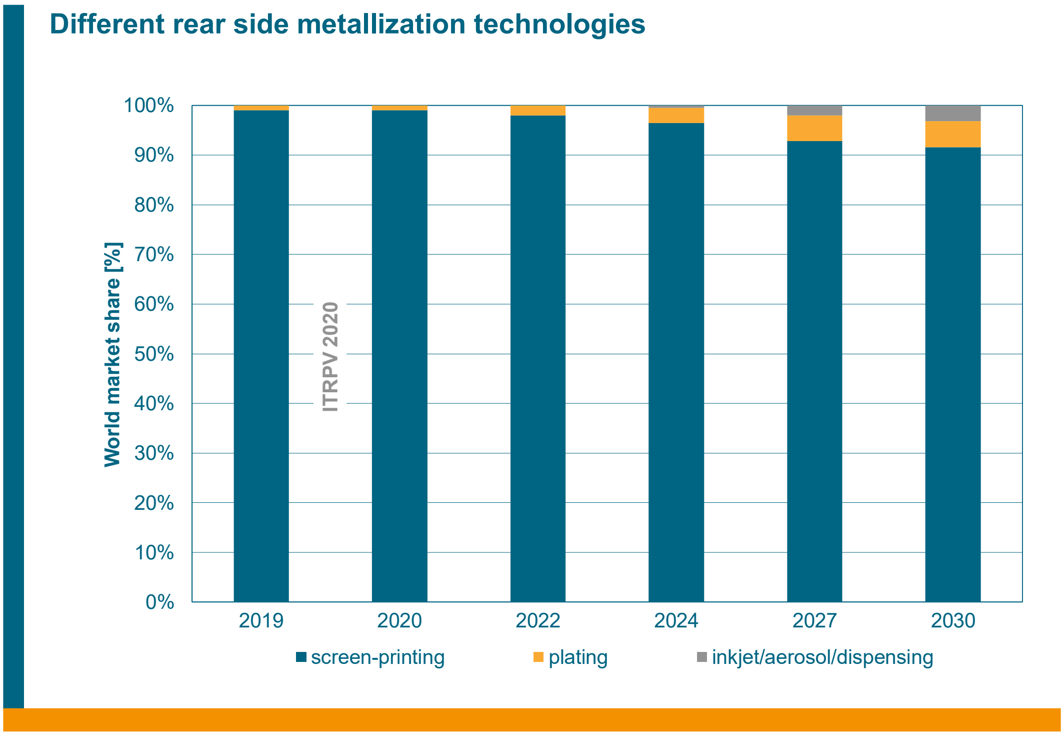


Fig. 36: Predicted trend for different rear side metallization technologies.

Optimizing productivity is essential to remain cost competitive. Increasing the throughput of the equipment in order to achieve maximum output is therefore a suitable way to reduce tool related costs per cell. In order to optimize the throughput in a cell production line, both, front-end (chemical and thermal processes) and back-end (metallization and classification) processes should have equal capacity. In former editions of the ITRPV we considered two scenarios: an evolutional optimization approach to optimize existing tool sets and a progressive scenario, for trends of new equipment's, with higher process throughputs. As discussed in chapter 5.3., we currently see the trend to larger wafer formats. Existing cell fabs will not be upgraded for wafer formats of ≥ 166 mm² x 166 mm² as shown in Tab. 1.

Therefore Fig. 37 summarizes the expected throughput of new cell production equipment, until 2030. New lines for PERC will be equipped from the beginning with new tool concepts that matured during the last years in newly built production lines. Metallization tools with throughputs of ≈7.000 wafers/h are available on the market today. Further improvements in this field will depend strongly on the progress made with the screen-printing technology that currently focuses on smaller line width and lower paste consumption. Wet chemical processing is leading with 8.000 wafers/h today and is expected to continue leading the throughput per tool with up to 15.000 wafers/h by 2030 as well. A maximum of ≈10.000 wafers/h is expected by 2022 for metallization and test equipment. Thermal processing is expected to somewhat lag behind in terms of throughput. So innovative equipment/process solutions for increased throughput in thermal processing are required.

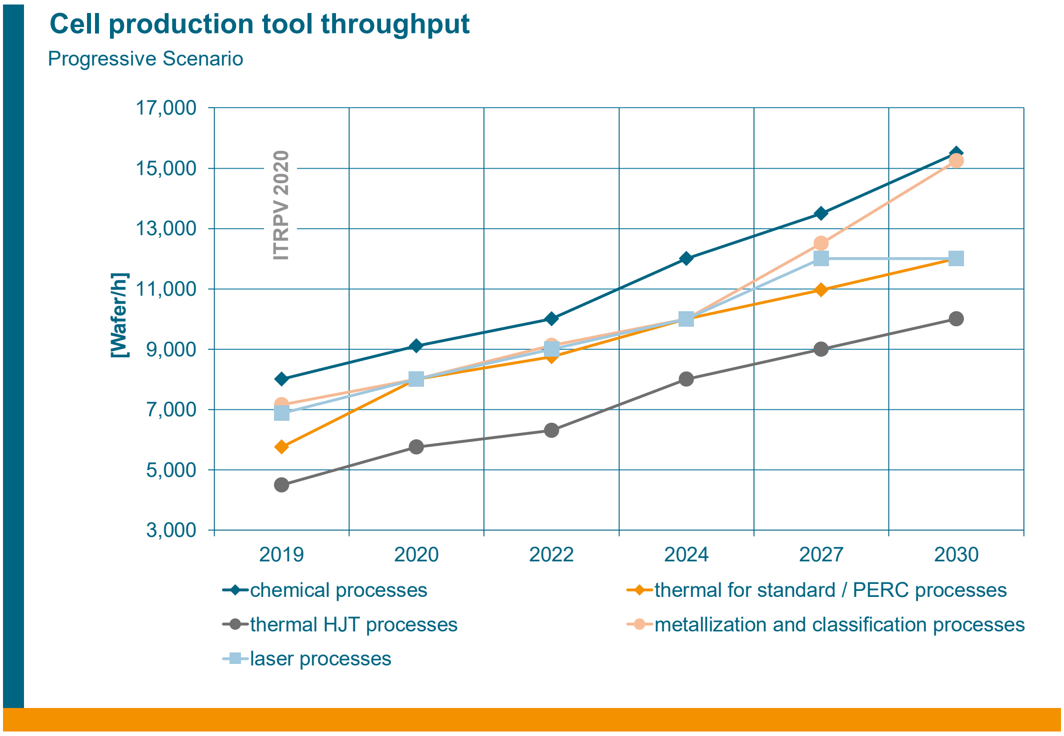


Fig. 37: Predicted trend for throughput per tool cell production tools.

6.3. Products

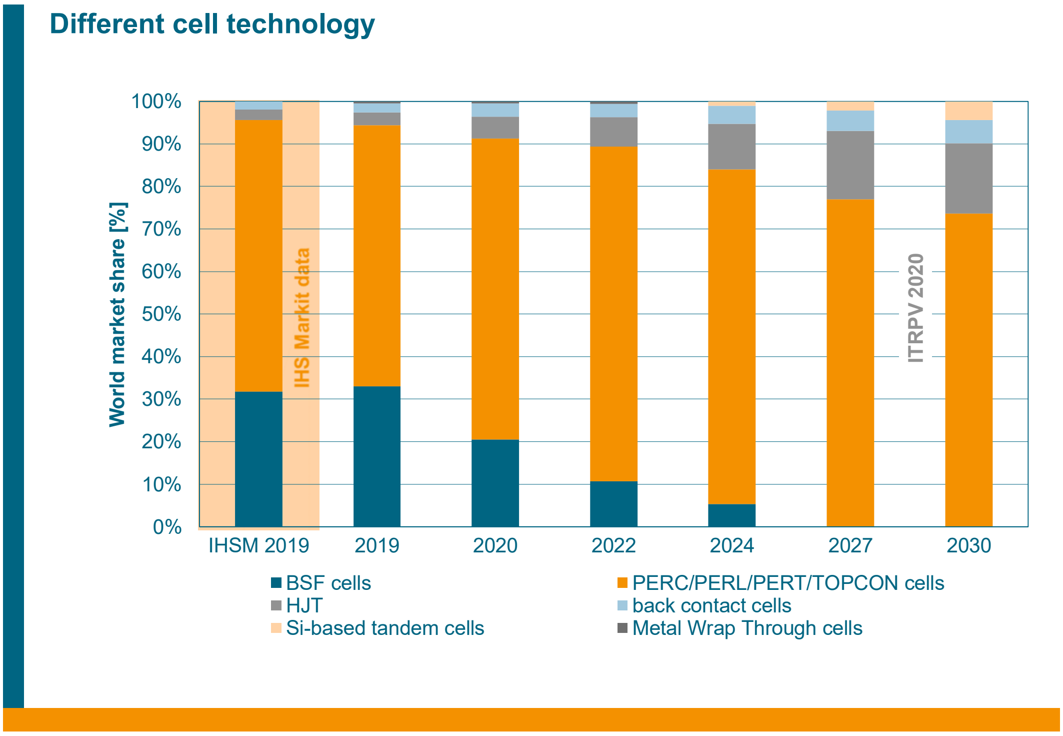


Fig. 38: Worldwide market shares for different cell technologies. IHS Markit data are indicated for 2019 as reference for 2019 [19].

We found for 2019 a share of about 30% for BSF and more than 60% for cell concepts with diffused and passivated pn-junctions and passivated rear sides (PERC/PERL/PERT/TOPCON). This is in line with IHS Markit assumptions as shown in Fig. 38 [19]. PERC/PERT/PERL will dominate the market over the next years. HJT cells are expected to gain a market share of about 10% in 2024 and 17% by 2030.

Fig. 38 confirms again the market dominance of double-sided contact cell concepts. Rear-side contact cells are not expected to have significant market share: we assume a change from ≈2% in 2019 to nearly 5% in 2030. Si-based tandem cells are expected to appear in mass production after 2022, again a delay compared to last ITRPV editions. BSF is assumed to be produced mainly on cost efficient mc-Si and will probably disappear after 2024.

Fig. 39 highlights trends in cell technologies with passivated, diffused pn-junction on the front side and passivated rear side. There are different approaches to realize such cells. The most common approach uses p-type material with a passivating layer of Al_2O_3 and a SiN_x capping layer as discussed in chapter 6.2. In 2019 about 15% of PERC cells were produced in this technology with p-type mc-Si material, 80% were PERC on p-type mono-Si. This share is expected to stay stable in 2020 and it will decrease to about 60% within the next 10 years. PERC on n-type material is expected to have a small market share below 5% over the next years. PERC on mc-Si material will fast lose market share. New concepts on n- and p-type material with passivated contacts using tunnel oxide passivation stacks at the rear side will gain market share in 2020 - expectation is that the share will increase close to 40% within the next years.

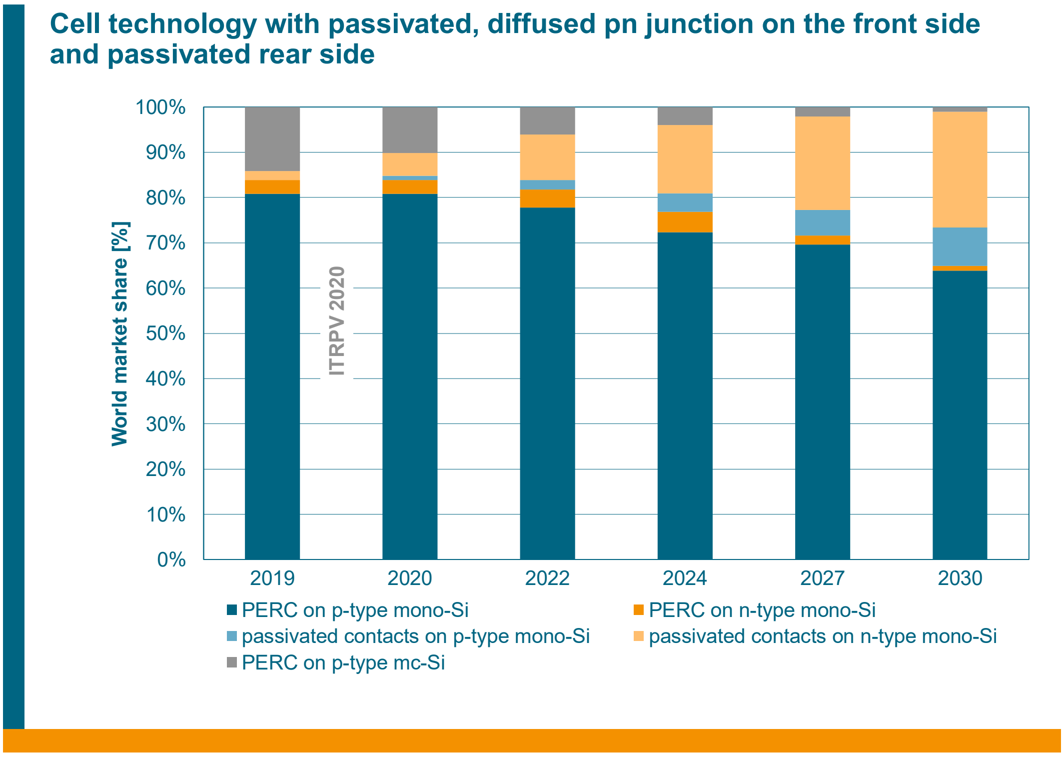


Fig. 39: Worldwide market shares for c-Si cell concepts with pn-junction on the front and different rear side passivation technologies.

We estimate that the majority will use n-type bulk material and a much smaller share will deploy p-type material. All cell types discussed in Fig. 39 as well as HJT cells can trap the light from the front and from the rear side if the electrical contacts are designed accordingly. This cell types can be used for bifacial light capturing. Fig. 40 shows the expected market trend for bifacial cells. The 2019 market share of about 20% in 2020 is expected to increase significantly to 70% within the next 10 years.

Bifacial cell in world market

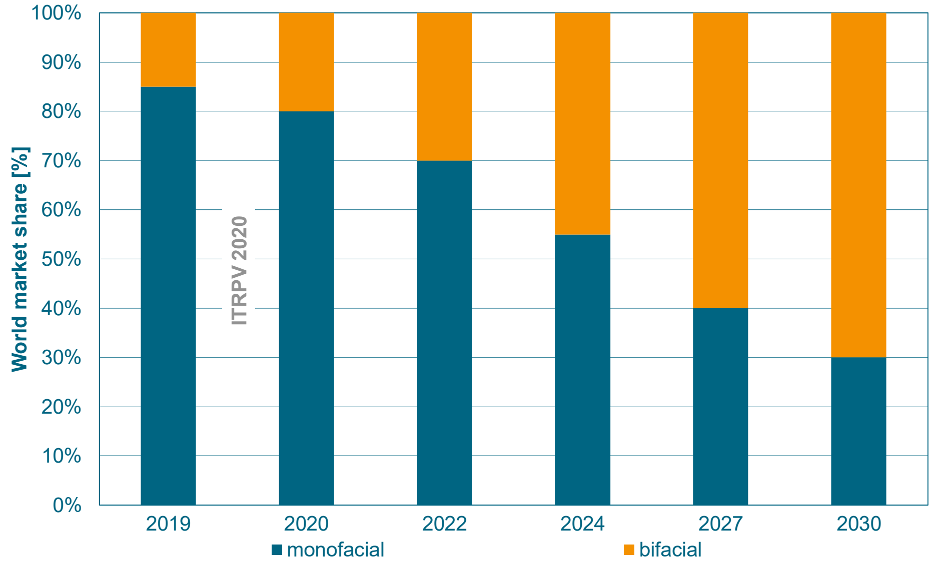


Fig. 40: Worldwide market shares for bifacial cell technology.

Fig. 41 shows the expected average stabilized front-side cell efficiencies of state-of-the-art mass production lines for double-sided contact and rear-contact cells on different wafer materials. The plot shows that there is potential for all technologies to improve their performance. Tandem cells are considered for the first time.

Average stabilized efficiency values for Si solar cells in mass production

(158.75x158.75mm²) measured with bus bars (no BB-less measurement) and front side STC

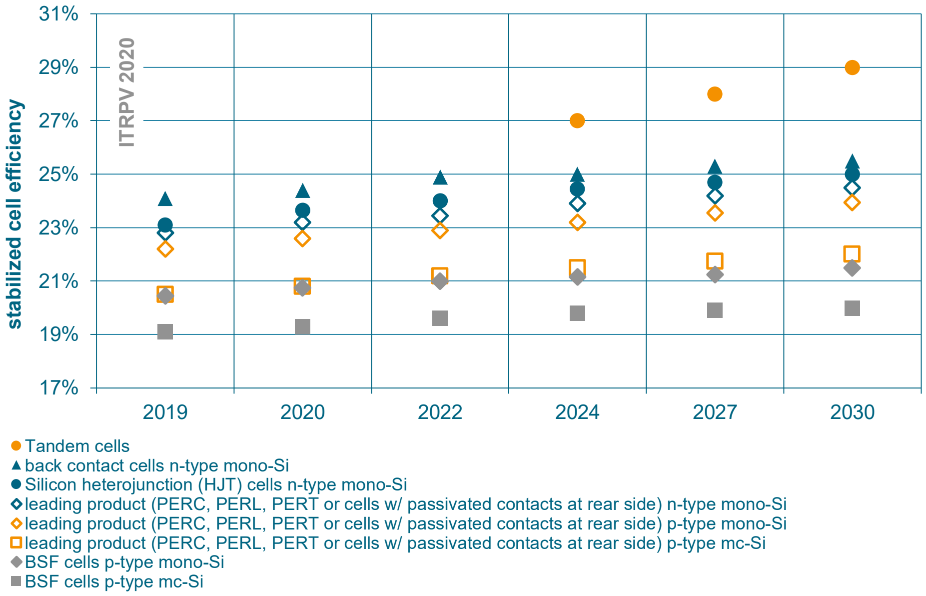


Fig. 41: Average stabilized efficiency values of c-Si solar cells in mass production (158.75 x 158.75 mm²).

According to the findings, as shown in Fig. 41, we expect cells with efficiencies of ≥ 27% in mass production from 2024 onwards. N-type cells show the highest efficiency potential of today's cell technology concepts. N-type cells with diffused pn-junction and passivated rear side are expected to show a higher efficiency potential than p-type cells. This is mainly due to the expected introduction of passivated contact cell concepts as shown in Fig. 39. We found that p- and n-type mono-Si cells will reach 24% and 24.5% in 2030, respectively. Other n-type-based cell concepts like HJT and back-contact cells, will reach higher efficiencies of up to 25% and 25.5% respectively within the next 10 years and will approach record cell efficiencies for Si [25]. BSF cell technology is expected to reach an efficiency of up to 20% with mc-Si and 21.5% with mono-Si material.

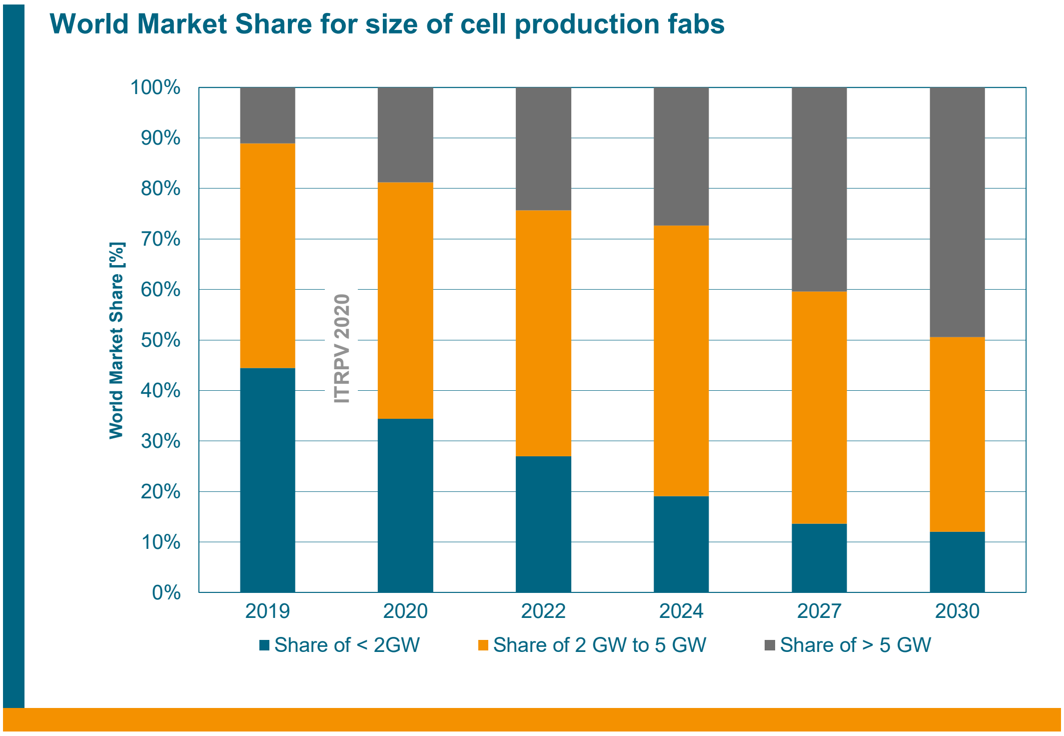


Fig. 42: Trend for name plate capacity of cell manufacturing fabs.

New built cell production facilities will make use of the economy of scale by increasing their annual production capacity. We find a dominating market share of factories with a production capacity between 2 and 5 GW. Fig. 42 shows that the share of fabs with > 5GW annual cell production capacity will increase in the next 10 years.

7. Results of 2019 | Module

7.1. Materials

Fig. 2 and Fig. 3 showed the price shares for mc-Si and mono-Si module products. The module related price share contributes with > 50% to the module sales price. Cells are still the most expensive part of the module's bill of materials (BOM). Module conversion costs are dominated by material costs. Improvements of the module performance and of material costs are therefore mandatory to optimize module costs. Approaches for increasing performance like the reduction of optical losses (e.g. reflection of front cover glass), reduction of resistance loss, and the reduction of interconnection losses will be discussed in chapter 7.2. Approaches for reducing material costs include:

- Reducing material volume, e.g. material thickness.
- Replacing (substituting) expensive materials.
- Reducing waste of material.

All non-cell module materials contribute to module manufacturing cost with a similar portion. The most massive material of a module is the front side glass. It mainly determines weight and light transmission properties. The thickness is also important regarding mechanical stability. Fig. 43 summarizes the trend in front side glass thickness. It is expected that a reduction to 2 mm thickness will appear over the next years. A thickness below 2 mm is expected to appear in the market from 2022 onwards with low market shares.

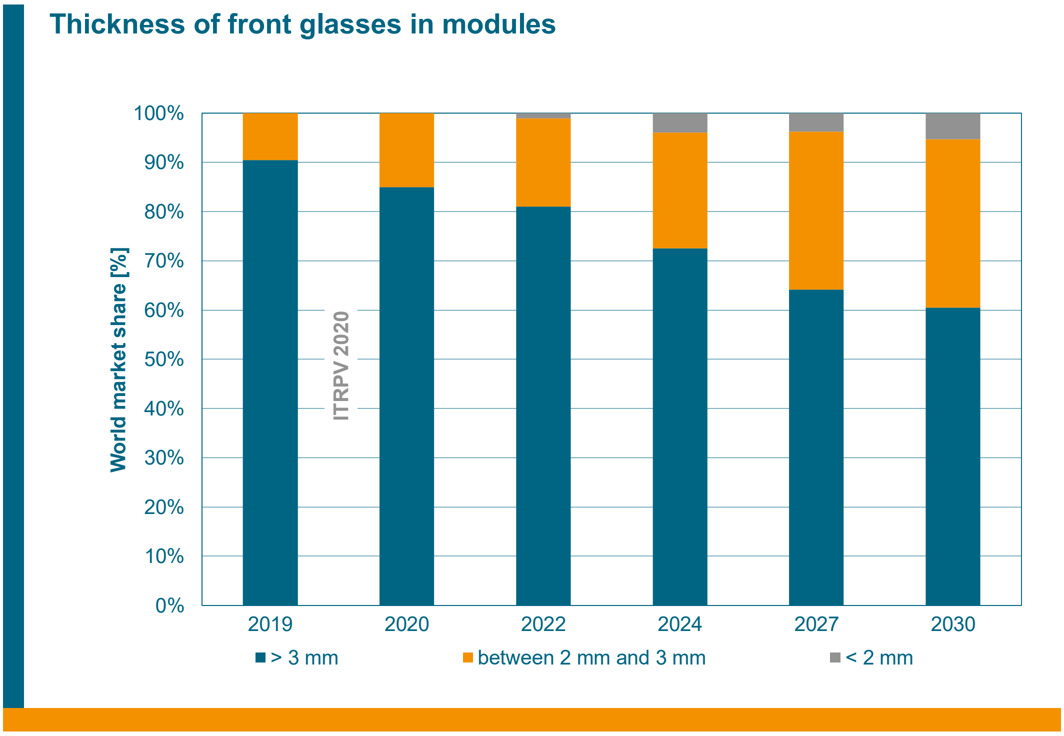


Fig. 43: Expected trend of front glasses in c-Si modules.

The use of antireflective (AR) coatings has become common to improve the transmission of the front cover glass. AR-coated glass will remain the dominant front cover material for c-Si PV modules in the future, with market shares well above 90%.

The transmission of AR coated glasses appears to be today around 94%, about 3% higher than for non-coated glasses. A continuous improvement of the glass is expected to reach up to 95.5% transmission within the next 10 years as shown in Fig. 44. Since AR-coated glass will be the most used front cover, it is important that the AR coating remains effective and stable under various outdoor conditions during the entire operational life of the module. All AR coatings on the market meet an average lifetime of at least 15 years, and, there is a clear trend indicating that the average service life of these coatings will improve to 25 years.

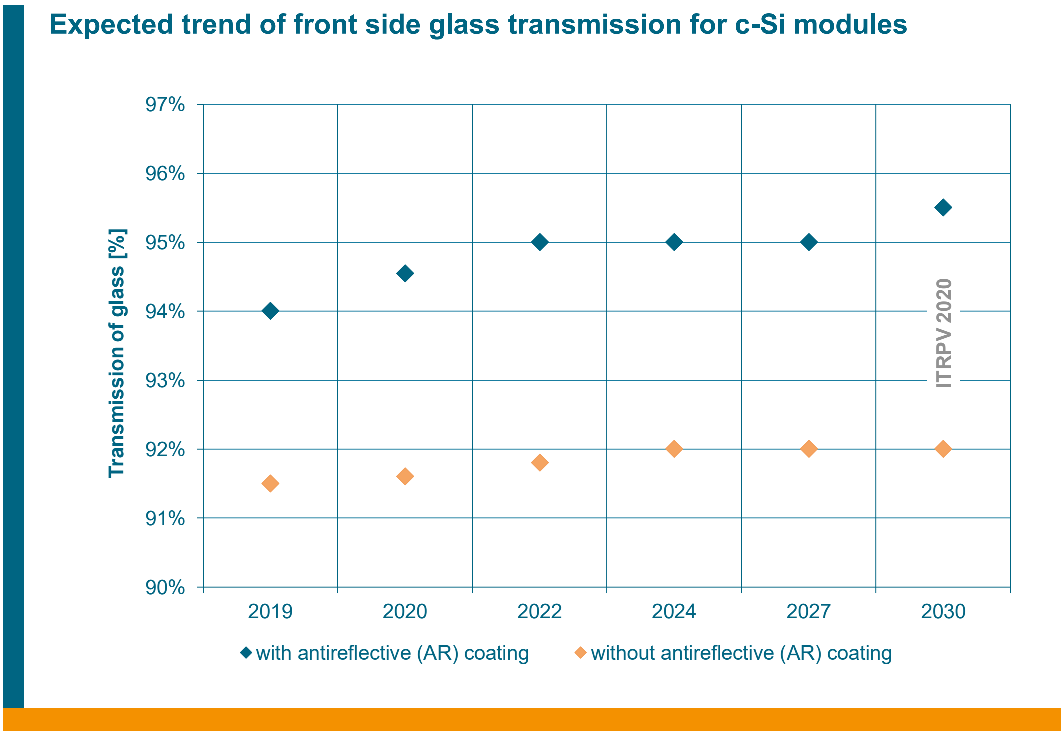


Fig. 44: Expected trend of front side glass transmission for c-Si modules.

Today, solders that contain lead are the standard interconnection technology for solar cells in module manufacturing. Due to environmental and other considerations as discussed in chapter 6.1, more PV manufacturers are striving towards lead-free alternatives, as can be seen in Fig. 45. Conductive adhesives are expected to gain after 2022 above 10%.

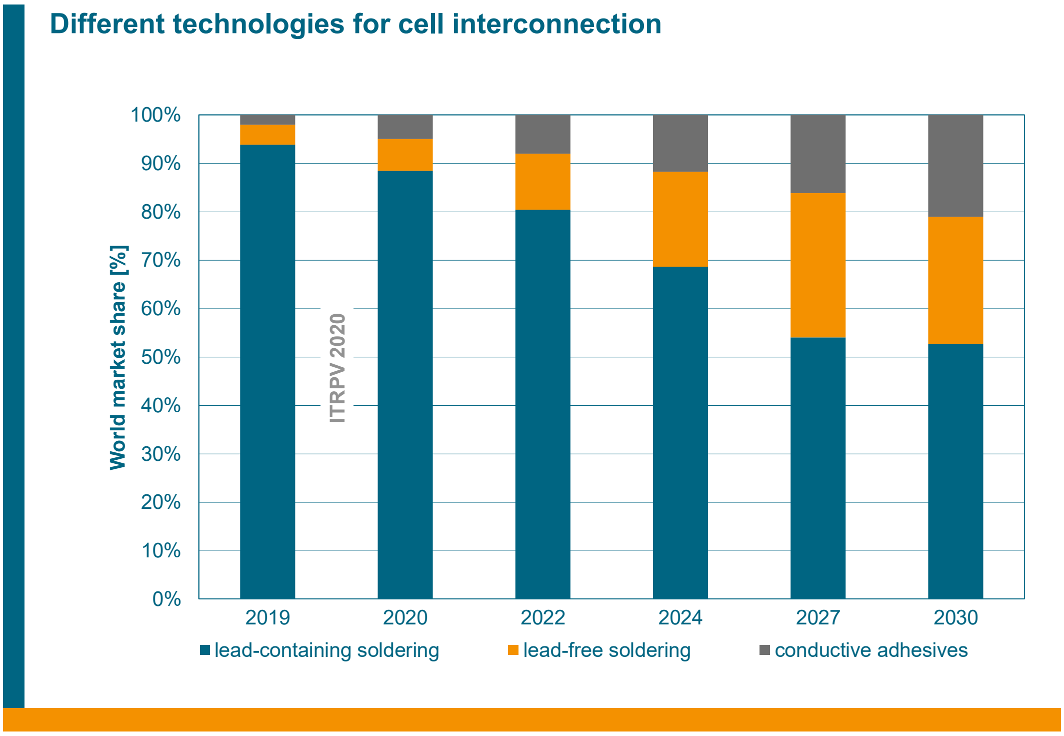


Fig. 45: Expected market share for different cell interconnection technologies.

As interconnector material, copper ribbons are today the dominating material as shown in Fig. 46. Copper wires will gain over 40% market share during the next years due to the success of half-cell technology. Overlapping interconnect technologies will also gain market share. Structured foils and non-Cu based ribbons are expected to stay at a market share of < 8%.

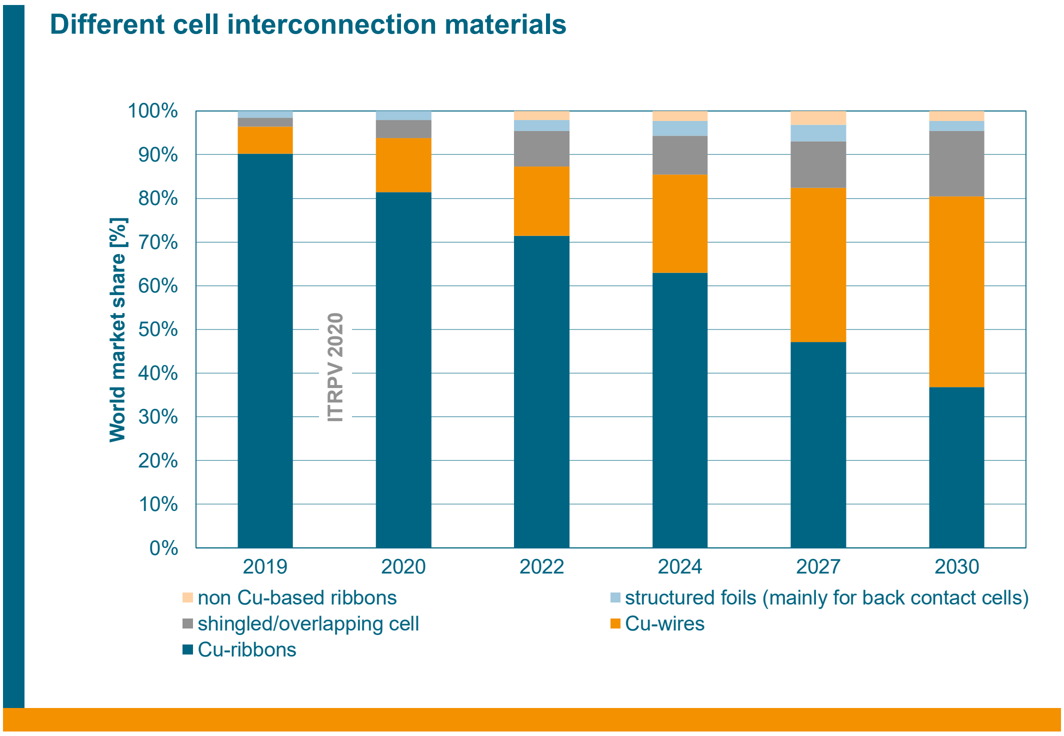


Fig. 46: Expected market shares for different cell interconnection materials.

It is important to note that the upcoming interconnection technologies will need to be compatible with the thinner wafers that will be used in the future. In this respect, low-temperature approaches using conductive adhesives or wire-based connections have an inherent advantage due to the lower thermal stresses associated with them.

Fig. 47 shows how module technology will be capable to process thinner cells as discussed in chapter 5.3. Cell thickness reductions, as shown in Fig. 12 and Fig. 13, will not be limited by module technology. So, Si material savings will contribute to future Wp cost reductions.

Similar to the cell interconnection we find a clear trend towards lead-free module interconnection covering all interconnections between the cell strings and the junction box, as shown in Fig. 48. Conductive adhesives and lead-free interconnects are available today and are expected to become dominating alternatives to currently used lead containing technologies.

The encapsulation material and the back sheet are key module components to ensure long time stability. Both are also major cost contributors in module manufacturing. Intensive development efforts have been made to optimize these components regarding performance and cost. Improving the properties of this key components is mandatory to ensure the module service lifetime. EVA will stay the most widely used encapsulation material for PV modules as shown in Fig. 49. Polyolefins are an upcoming alternative especially for bifacial products in glass-glass combination [26]. We expect an increasing market share for Polyolefins of up to 30% in 2030. Other materials are expected to keep low market share for niche applications.

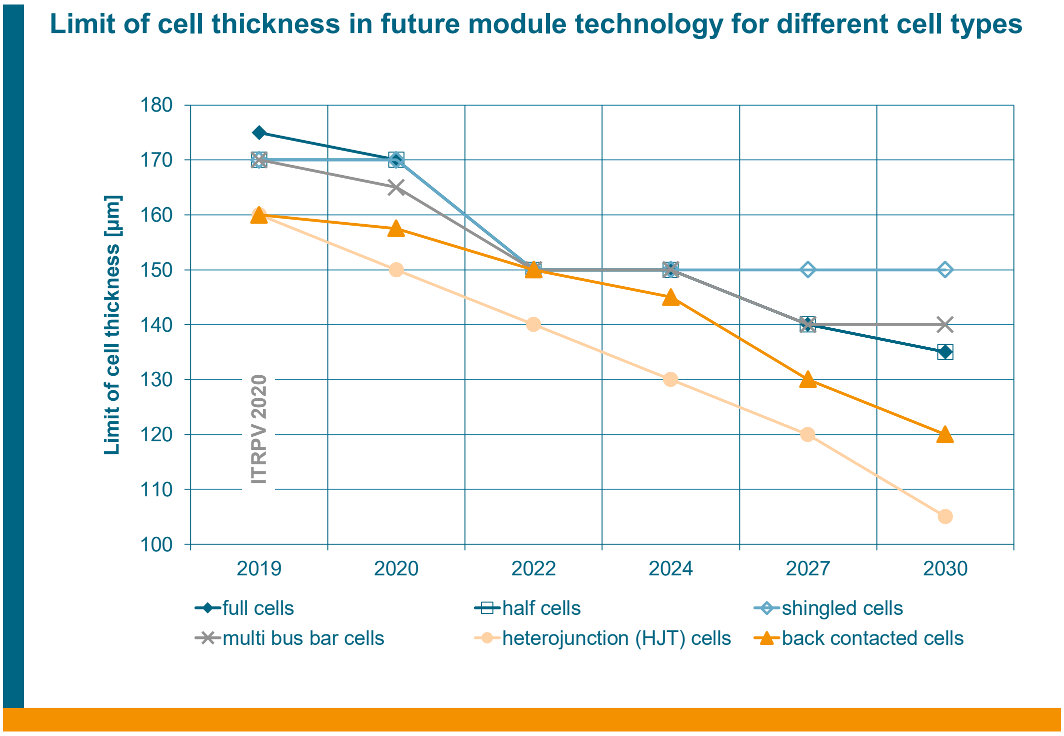


Fig. 47: Predicted trend of cell thickness limit in different module technologies.

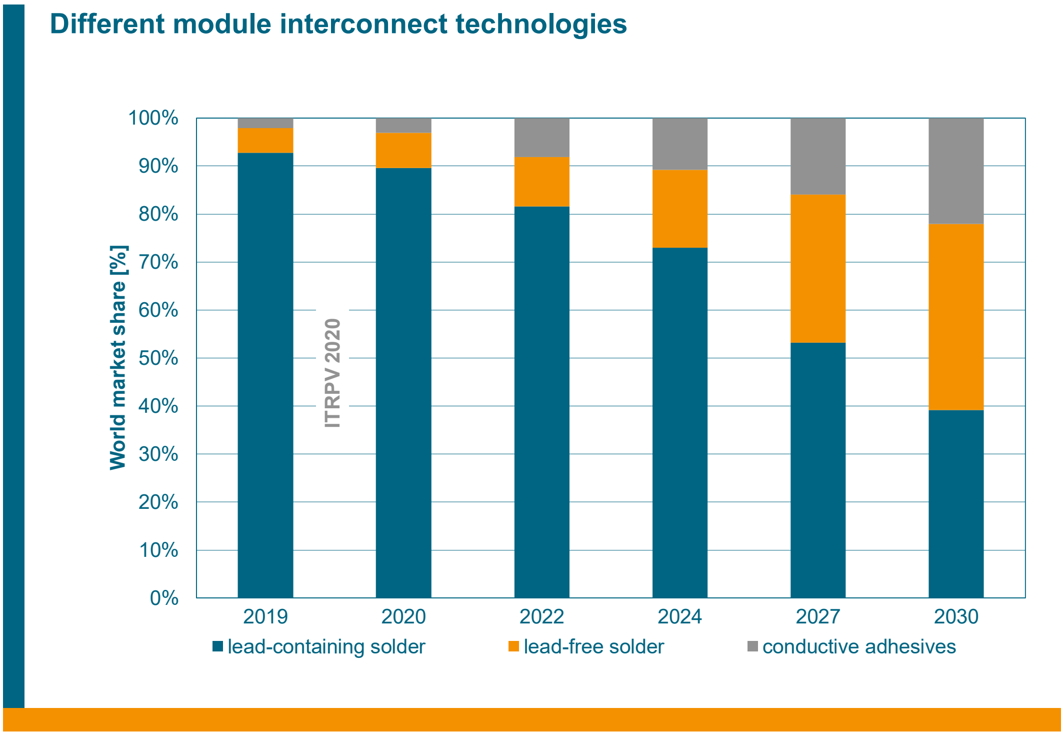


Fig. 48: Expected market share of different module interconnect technologies.

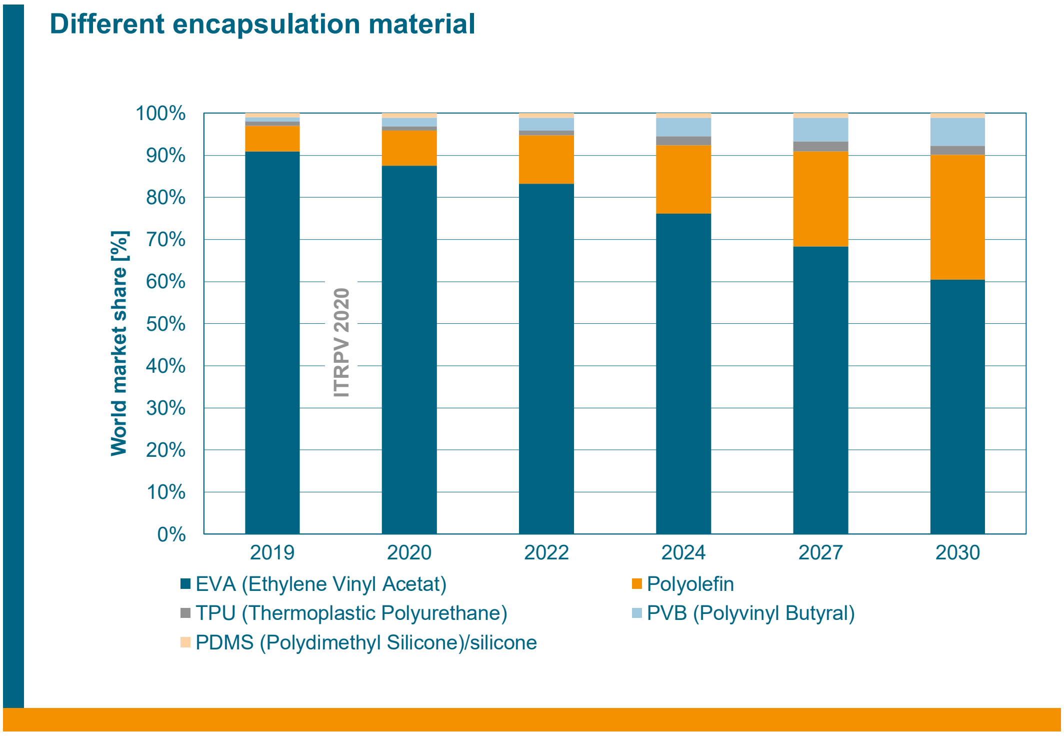


Fig. 49: Expected market shares for different encapsulation materials.

Fig. 50 shows the expected development in thickness of the different encapsulant materials. We see a clear trend to a considerable thickness reduction for all material types by up to 15% within the next 10 years.

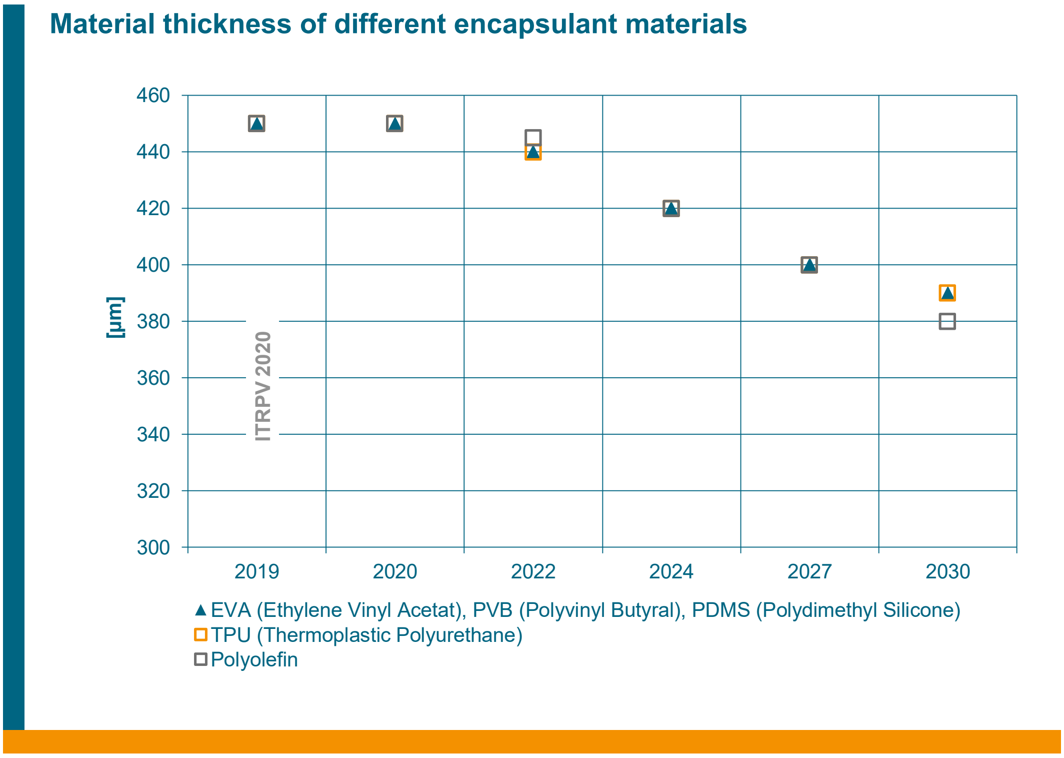


Fig. 50: Expected thickness reduction trend for different encapsulant materials.

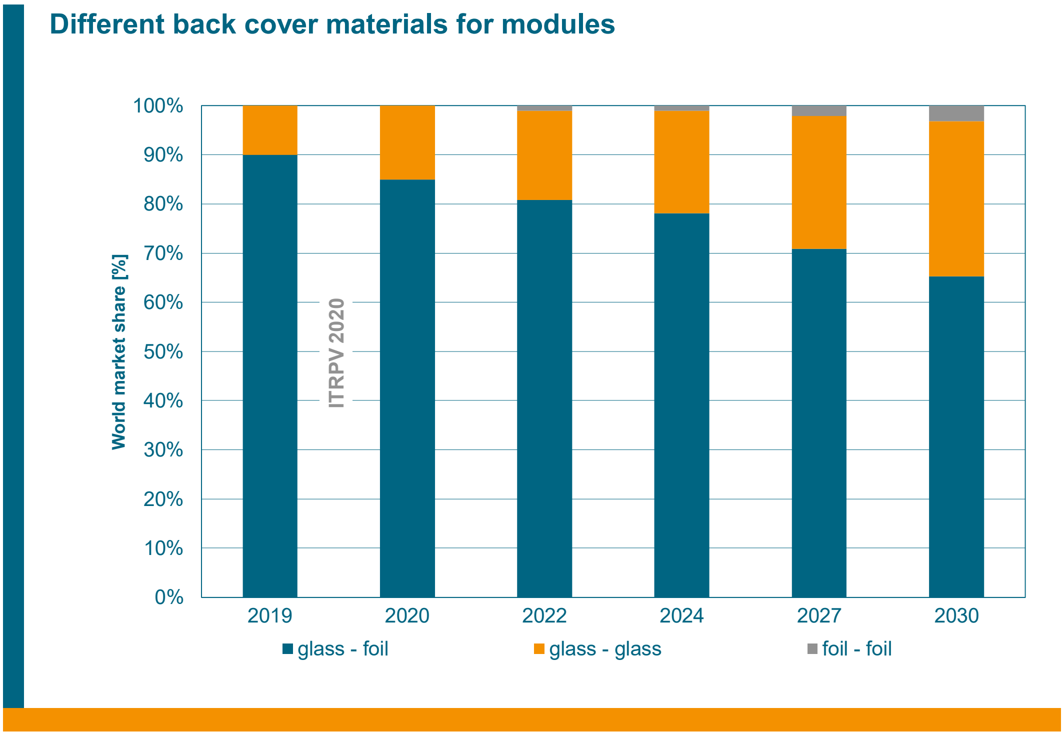


Fig. 51: Share of glass and foil as front and back cover.

As can be seen in Fig. 51, foils will stay mainstream as back cover material, but glass is expected to gain a significant higher market share as backside cover material especially for bifacial c-Si module applications to about 30% in 2030. Foil as front side cover will stay a niche. The thickness of the back glass is expected to stay in the range between 2 mm and 3 mm.

Fig. 52 summarizes the expected share of common backsheets. Polyethylene Terephthalate (PET) will stay in use as core layer for most of backsheet compositions as it provides good electrical insulation and protection against moisture. It is cost effective to produce. Numerous products use therefore PET as core layer, sandwiched between UV-protection layers [26]. Foils using Kynar (PVDF) are expected to keep the largest market share. Foils using Tedlar will have market shares between 15% and 25% while Polyolefin based backsheets will increase their market share and several new materials are expected to appear.

The mainstream color of the backsheet foils will stay white. Black colored backsheets will stay a niche application whereas transparent backsheets are considered as an upcoming trend - especially for bifacial cell applications as cost and weight efficient alternative to glass.

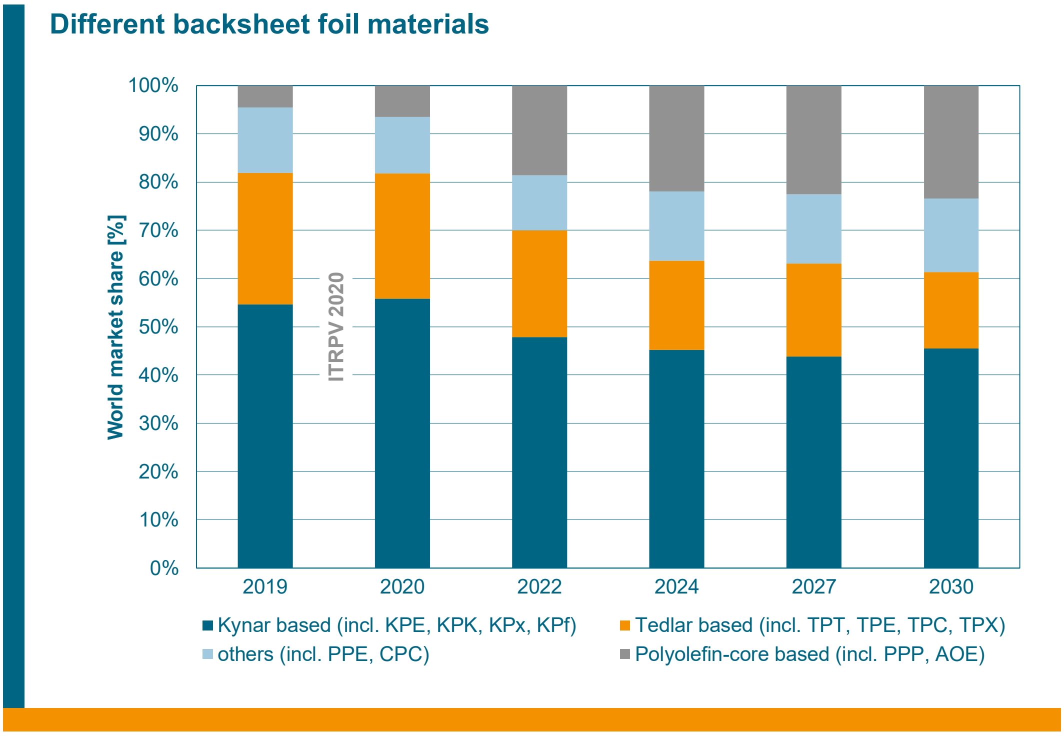


Fig. 52: Back cover foil materials trend: foils with PET core will stay dominant.

Fig. 53 looks at the trends for frame materials. Currently modules with aluminum frames are clearly dominating the market. Frameless modules are expected to increase its market share to about 20% in 2027. Plastics are considered as niche application with market shares of < 2%.

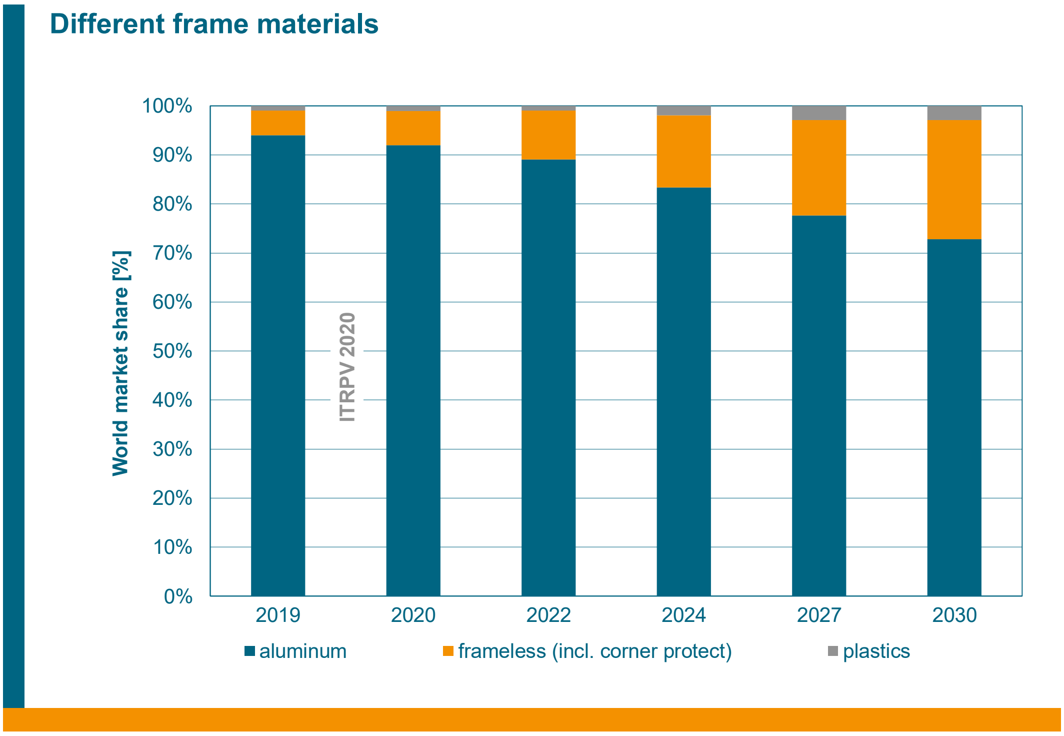


Fig. 53: Expected market shares for frame materials.

7.2. Processes

Increasing the tool throughput is also a measure for cost reduction in module manufacturing. The expected throughput trends of key equipment in module front end and back end are summarized in Fig. 54 , Fig. 55, and Fig. 56. We expect a continuous throughput increase in the next years. In 2030 the throughput of stringing tools is expected to increase to up to 130%.

In accordance to the disappearing of 3/4 BB 4BB stringers will not be improved as the arrow in Fig. 54 displays. The same will happen to 6BB from 2022 onwards. Stringing of half-cells require significant tool improvements as shown in Fig. 55.

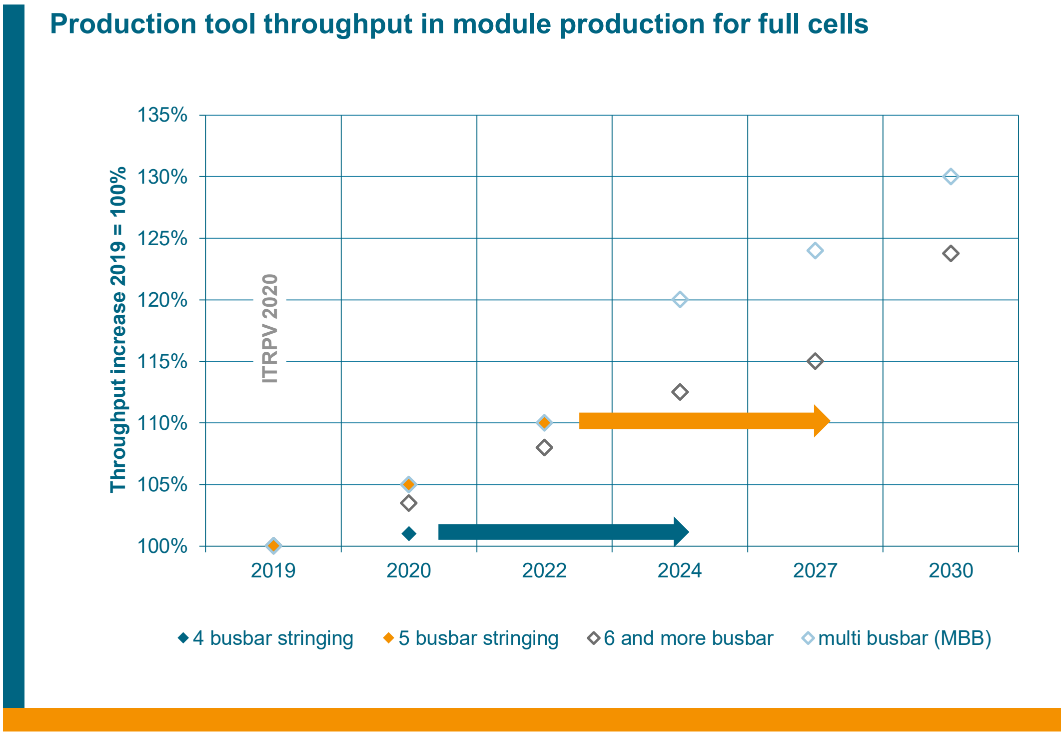


Fig. 54: Trend of tool throughput in stringing.

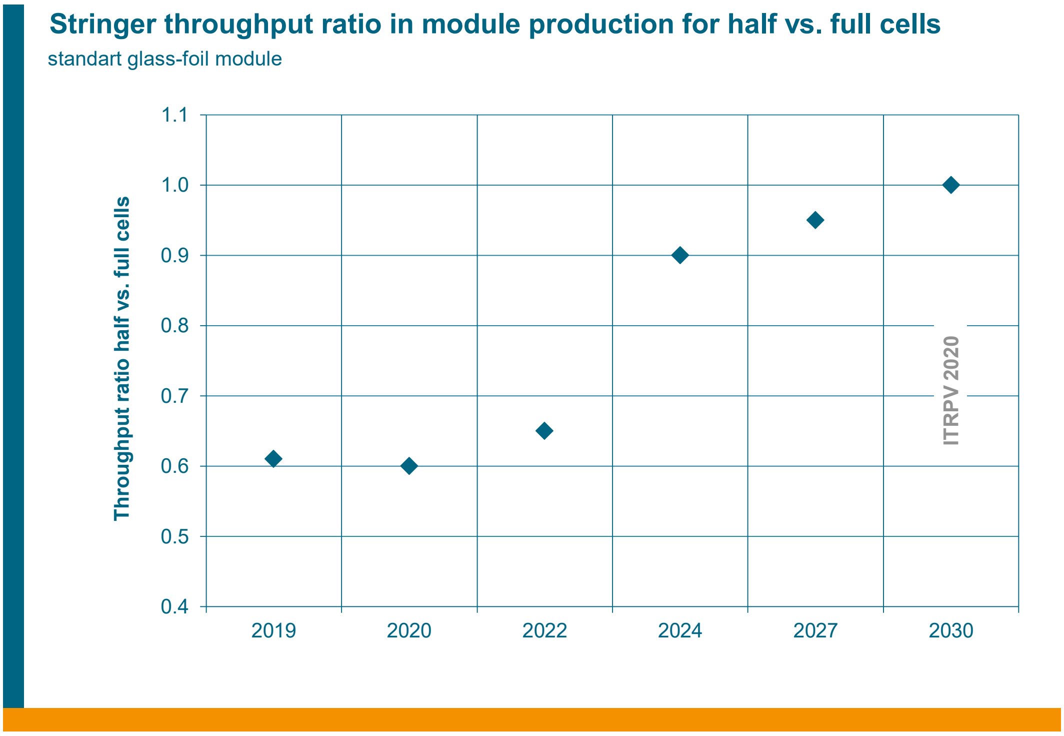


Fig. 55: Production tool throughput ratio of stringer in module production for half- vs. full-cell.

Fig. 56 shows the throughput trend for lamination. Glass-glass lamination will improve faster as it is currently behind glass-foil lamination throughput.

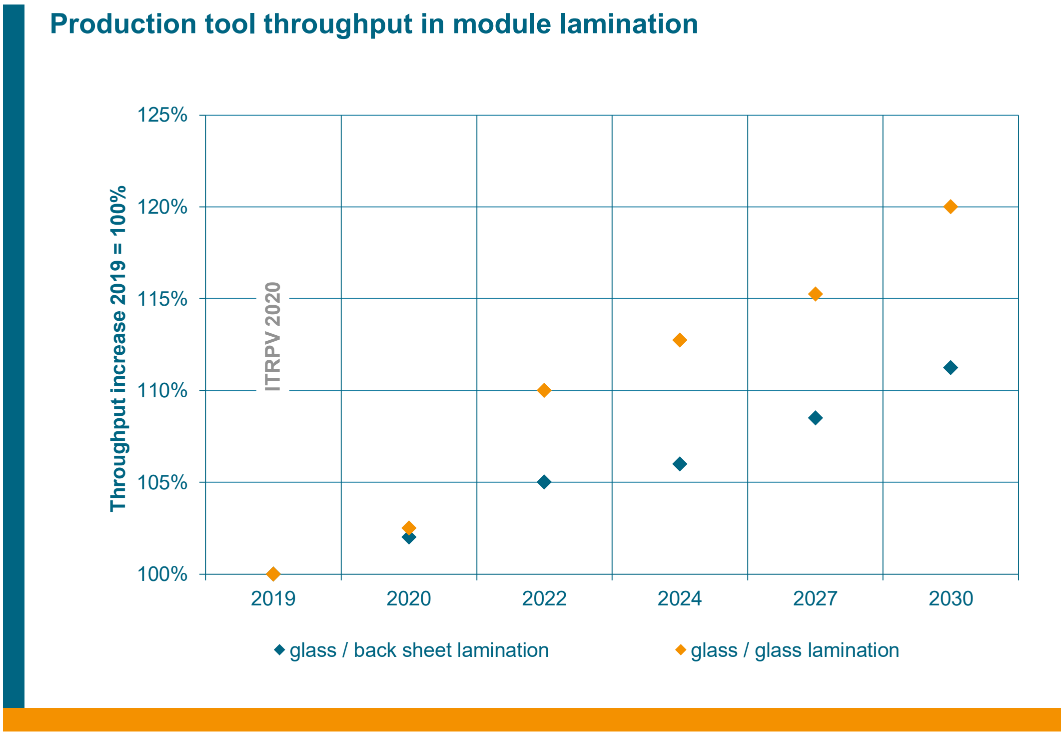


Fig. 56: Trend of tool throughput for module lamination.

In order to optimize the floor space utilization and hence the cost of module manufacturing, the equipment should occupy less floor space and achieve higher throughput. This should be possible by combining continuous improvements and new developments, particularly for connection and encapsulation processes. For the latter process, new encapsulation materials with shorter processing times would be desirable.

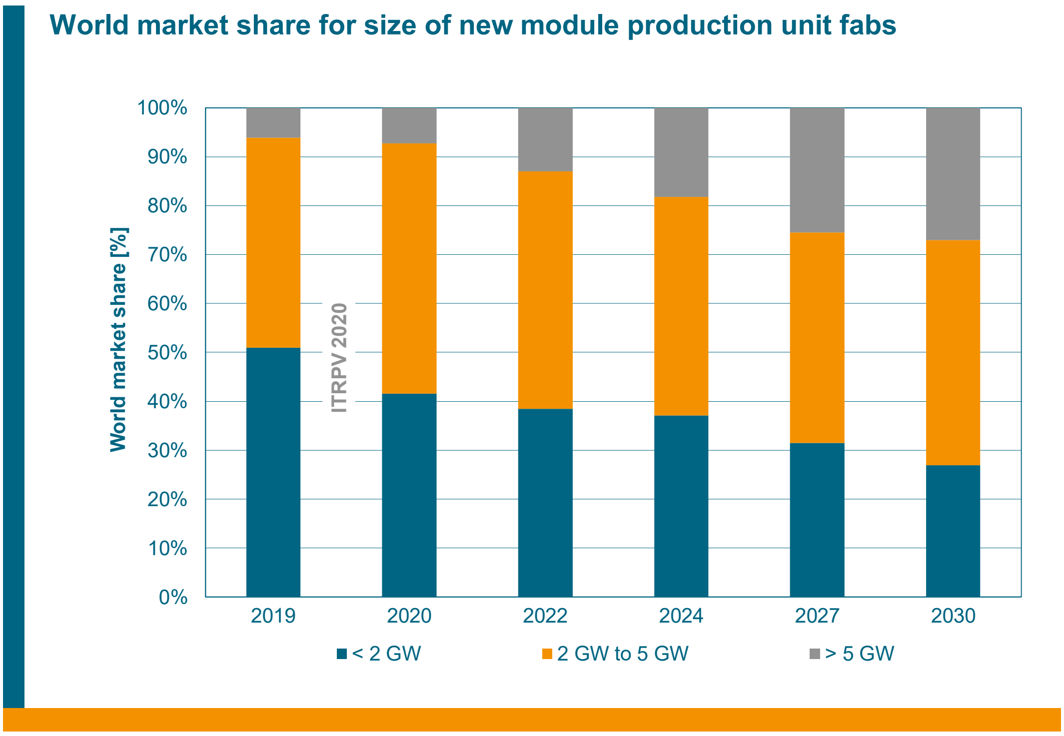


Fig. 57: Trend for name plate capacity of module manufacturing fabs.

The trend for module production fabs is like that in cell production as shown in Fig. 57. Factories with annual capacities of > 5GW will start dominating the production landscape. Nevertheless, smaller module fabs with < 2GW, down to 500MW are expected to be used for special applications and for special markets.

It is crucial to get as much power as possible out of the assembled solar cells. The cell-to-module (CTM) power ratio is a good parameter to describe this behavior. It is defined as module power divided by cell power multiplied by the number of cells (module power / (cell power x number of cells)).

Fig. 58 distinguishes in CTM between half-cell and full-cell applications. The CTM for full-cell modules was 2019 at 99% for mc-Si cell technology (acidic texturing) and at 98% for mono-Si cell technology (alkaline texturing), 101% and 100% respectively for the corresponding half-cell modules.

CTM exceeding 100% imply that the power of the finished module will exceed the power of the cells used in the module. Using of half-cell technology is one method to realize this. Smart interconnection techniques and further improvements of light management within the module as a mean of redirecting light from inactive module areas onto active cell areas are possible measures to improve the CTM.

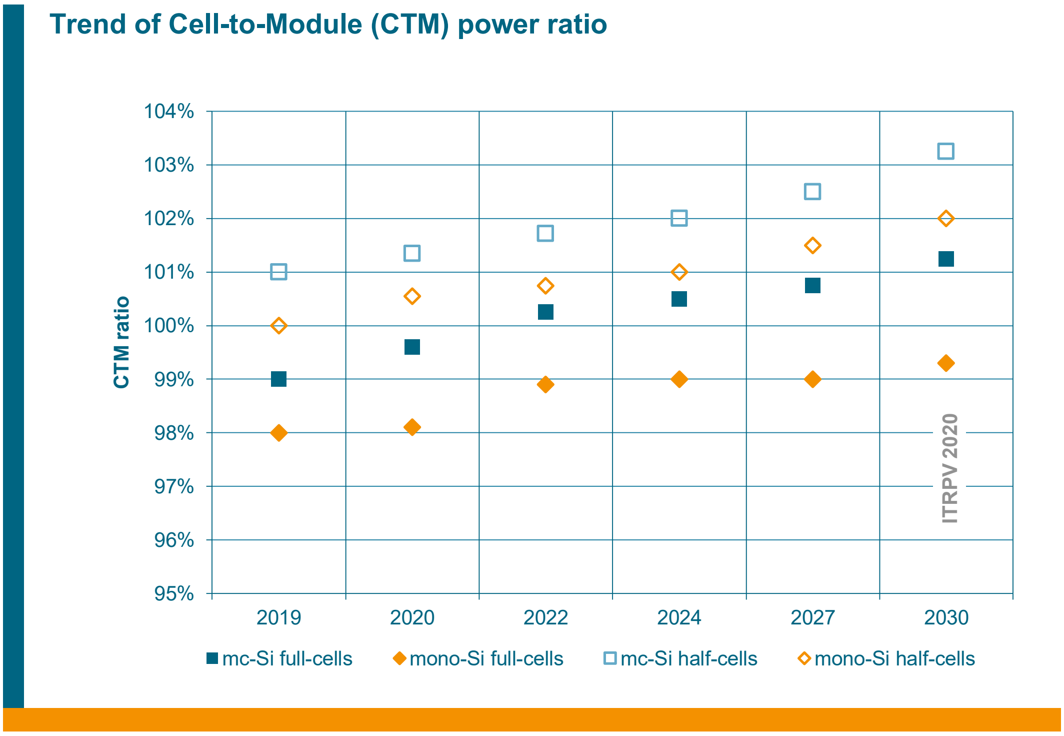


Fig. 58: Expected trend for the cell-to-module power ratio.

The introduction of new interconnection and encapsulation technologies (e.g. narrower ribbons, encapsulation materials with improved UV performance, etc.) will result in further improvements that will enable additional power gains but reduction of CTM. CTM, finally will stay a good parameter to monitor the process stability of the module production process.

7.3.Products

Due to the current diversification in wafer formats as discussed in chapter 5.3., also module dimensions are changing. Comparing different module types only by the so far common module label power may be misleading as module powers with ≥ 500 W are possible with existing cell technologies [21, 22]. Therefore, the module area efficiency is a useful parameter to compare different technologies. Module area efficiency is calculated by the module label power divided by module area in m² (module power / module area). In today's module data sheets, the module efficiency is indicated - a value of 20% corresponds to a module area efficiency of 200 W/m².

Fig. 59 shows the expected trend of average module area efficiency for modules in mass production with different cell technologies.

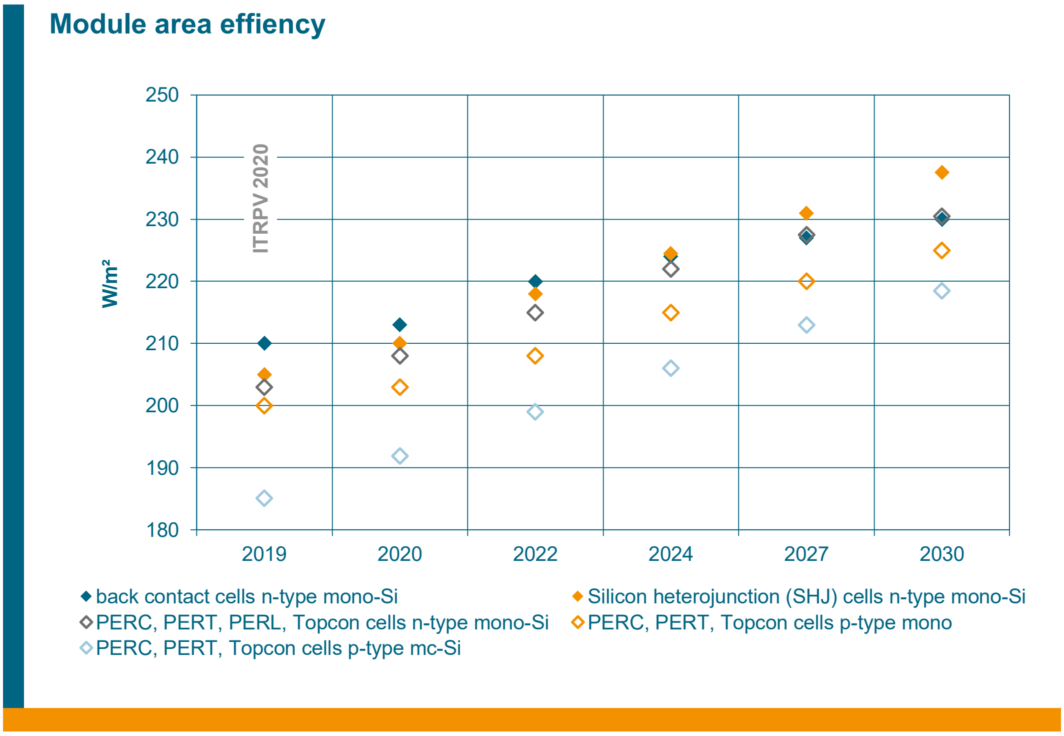


Fig. 59: Average module area efficiency in mass production for different c-Si solar cell technologies.

The expected area efficiency for mc-Si based products will stay below mono-Si based technologies. Current PERC p-type mono-Si modules are expected to show area efficiencies of 203 W/m² in 2020 and up to 225 W/m² in 2030. Modules with n-type cell concepts, especially with tunnel oxide passivation technologies, are expected to be ahead of p-type PERC with 208 W/m² in 2020 and with up to 230 W/m² in 10 years. In 2020 HJT modules reach 210 W/m² and are expected to outperform other c-Si module types with 238 W/m² in 2030.

Fig. 60 and Fig. 61 show the calculated module power trend of modules with typical dimensions of 1.7 m² for 120 half-cell and of 2.0 m² for 72 full-cell / 144 half-cell respectively, using 158.75 x 158.75 mm^2 cell format and efficiencies shown in chapter 6.3., Fig. 41 and the cell-to-module power ratios are shown in Fig. 58.

Modules with high efficiency back-contact cell technology in 158.75 x 158.75 mm² format have not been available in the market yet, therefore we consider in Fig. 60 and Fig. 61 the calculated power classes for double-side contact c-Si technologies only to stay comparable.

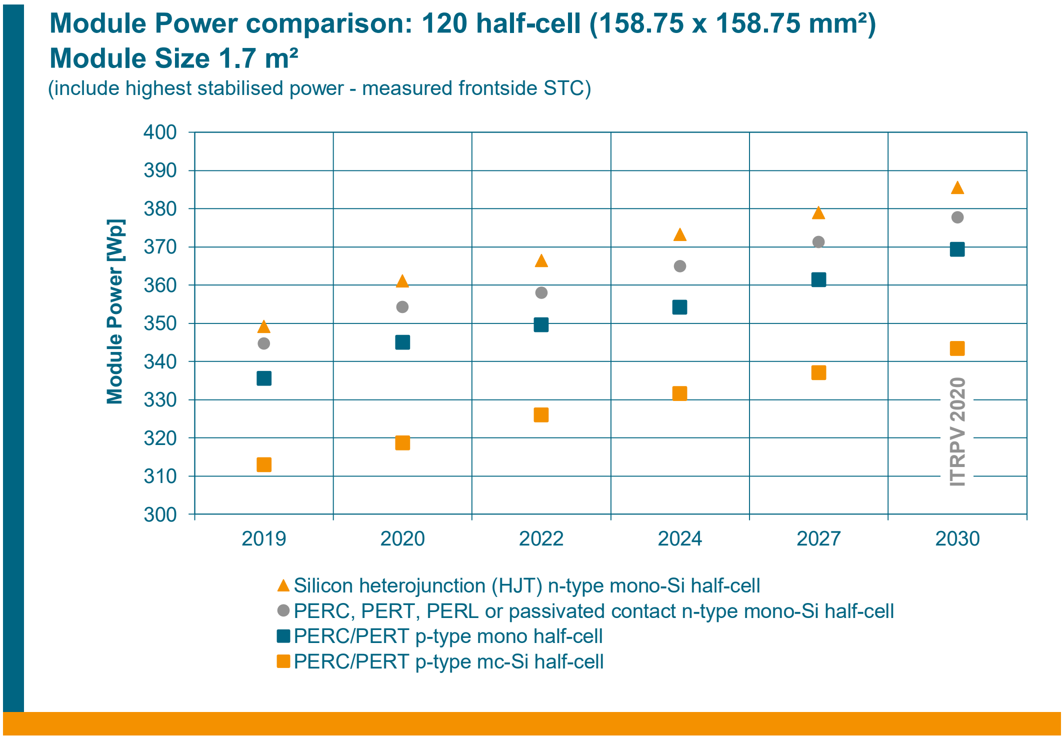


Fig. 60: Predicted trend curve for module power for moduels with 1.7 m² area for different c-Si celltechnology types.

Modules with about 1.7 m² will be used in applications with area limitations like roof top installations. In Fig. 60 we therefore show the expected module power trend for double-side contact cell with half-cell technology - it enables highest power classes in this format. Modules with mc-Si PERC half-cells will achieve module power classes of ≈345 W by 2030.

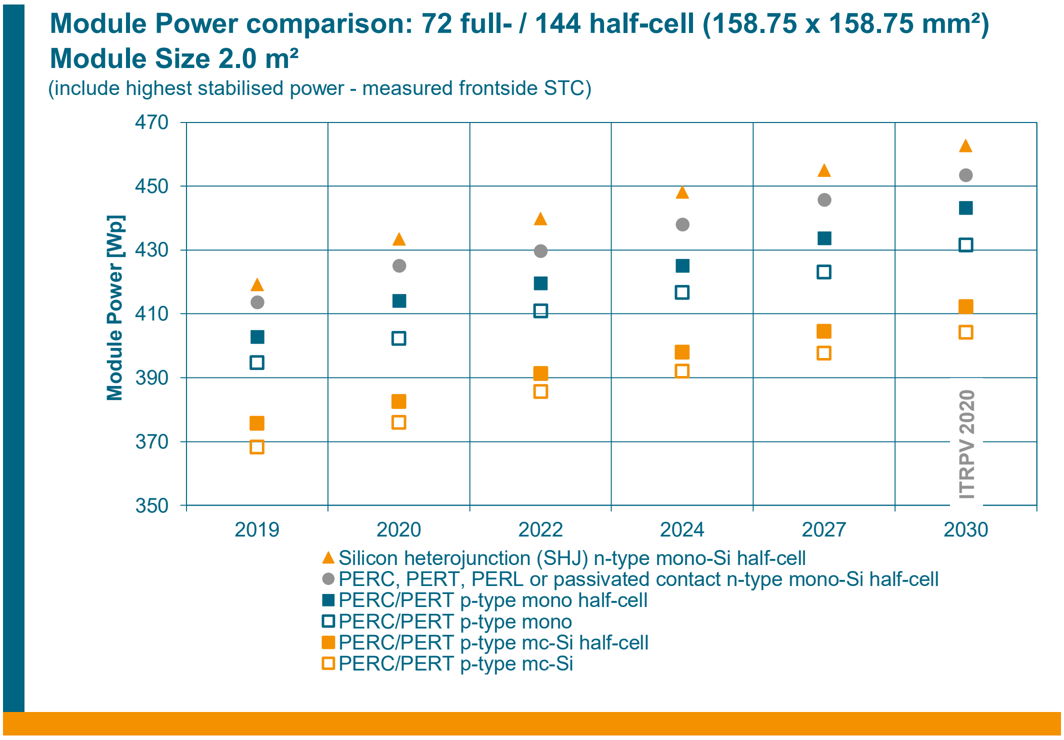


Fig. 61: Predicted trend curve for module power of modules with 2.0 m² area for different c-Si cell technology types.

Modules with mono-Si p- and n-type PERC cells have 345 W in 2020 and will achieve a power output of 370 W for p- type and close to 380 W for n-type by 2030, as shown in Fig. 60. Modules with HJT cells of this cell format show 360 W in 2020 and will reach 385 W in 2030. Using larger cell formats like M4 or M6 will result in higher module power classes but with larger modules areas.

The calculated corresponding module power of modules with around 2 m² area is shown in Fig. 61. This format utilizes typically 72 full-cells or 144 half-cells and is widely used for applications with no area limitation like power plant installations. Modules with p-type PERC cells will surpass in 2030 400 W for mc-Si and 430 W for mono-Si. N-type cells with tunnel oxide passivation will enable power classes up to 450 W in 2030. HJT modules show the highest module power for double-sided contact cell concepts.

Modules using half-cell technology were introduced in the market in order to reduce interconnection losses and therefore improving the area efficiency and the module power as shown above. Since this technology requires an additional process step for cutting the cells as well as a modification of the stringer equipment and reduction of the stringer throughput as shown in Fig. 55, it has an impact on the module manufacturing process. Nevertheless, the benefit in module power is remarkable as illustrated by direct comparison of different p-type PERC products in Fig. 61.

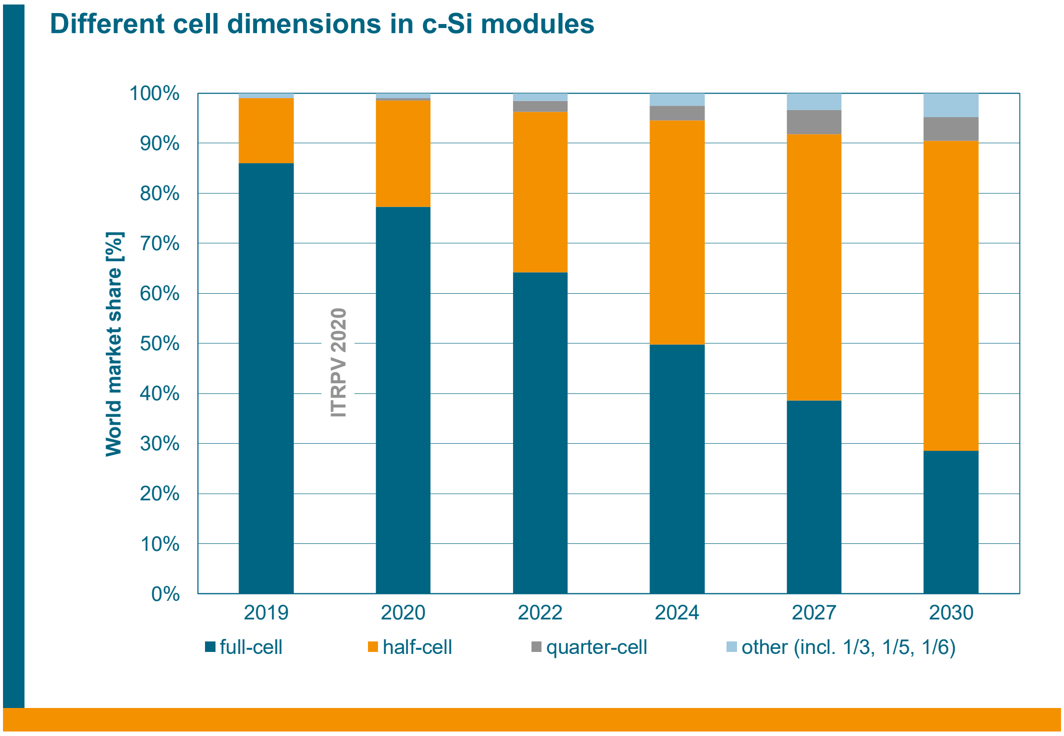


Fig. 62: Predicted market shares for modules with full-, half-, and quarter-cells; other inlcudes 1/3, 1/5, 1/6 for 210 x 210 mm².

Fig. 62 shows the expected market share of different cell dimensions in c-Si modules. Due to the better CTM performance and resulting in higher module efficiency, the share of half-cells will continue to grow from about 20% in 2020 to > 60% in 2030. In addition, we expect the appearance of modules with quarter cells after 2021.

Fig. 63 shows that the module market splits into two main sizes: 60 full-cell / 120 half-cell and 72 full-cell / 144 half-cell modules. Smaller and larger modules are for special markets. The larger module sizes are mainly used in utility applications. Other module dimensions for niche markets are expected to account only for less than 10% of the market during the next years. Today's mainstream modules (60 full-cell / 120 half-cell) will lose market share from today > 50% to about 35% in 2030.

Different module sizes

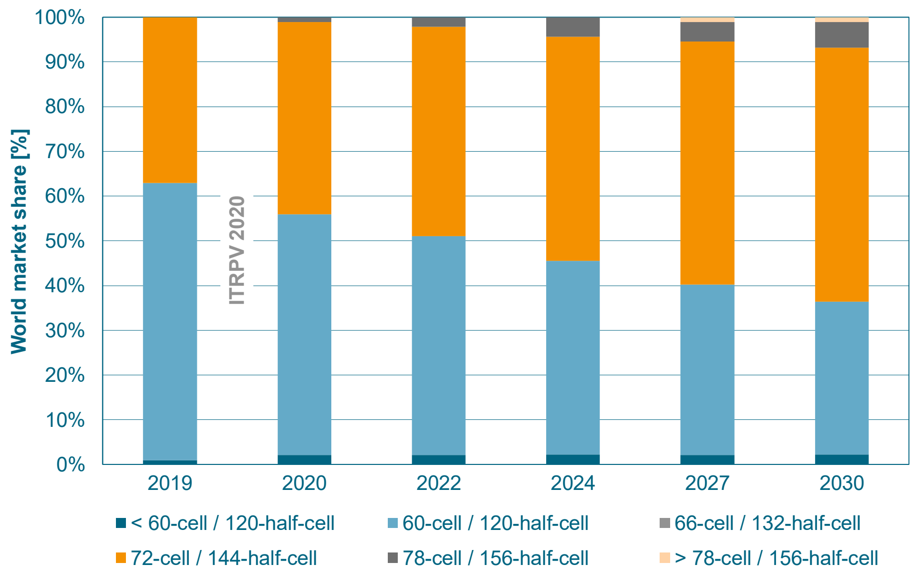


Fig. 63: Market shares of different module sizes with 158.75 x 158.75 mm² cells.

Bifacial Module Technology

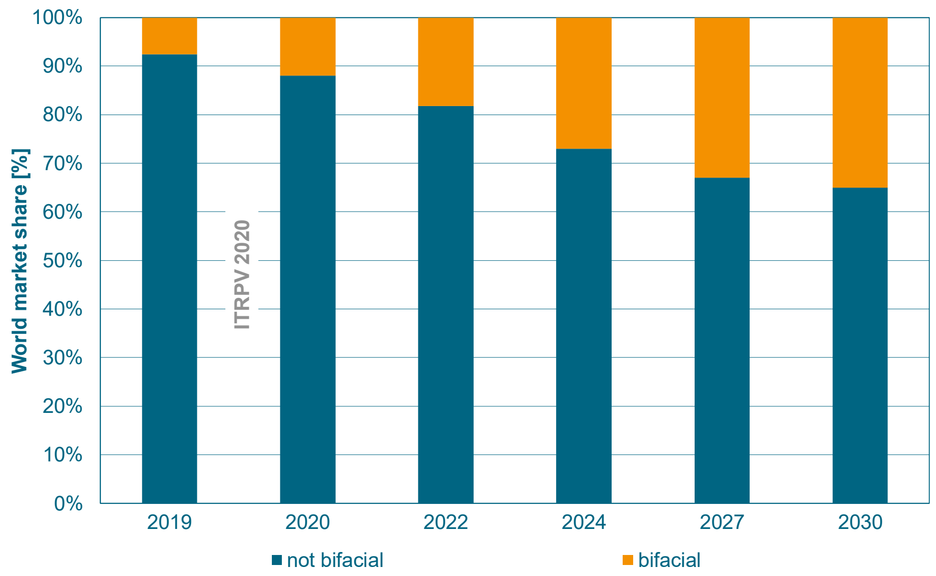


Fig. 64: Market share of bifacial modules.

Today most of modules are still monofacial modules. Bifacial cells can be used in bifacial modules as well as in conventional monofacial modules. As discussed in chapter 6.3 and shown in Fig. 40 bifacial cells will gain market share. We expect, that between 50% and 60% of bifacial cells will be assembled in bifacial modules and the remaining 40% -50% will be used in monofacial modules.

We therefore anticipate that the market share for bifacial modules will increase from 10% in 2020 to at least about 35% in 2030 as shown in Fig. 64. Bifacial modules will mainly be developed in power plant installations.

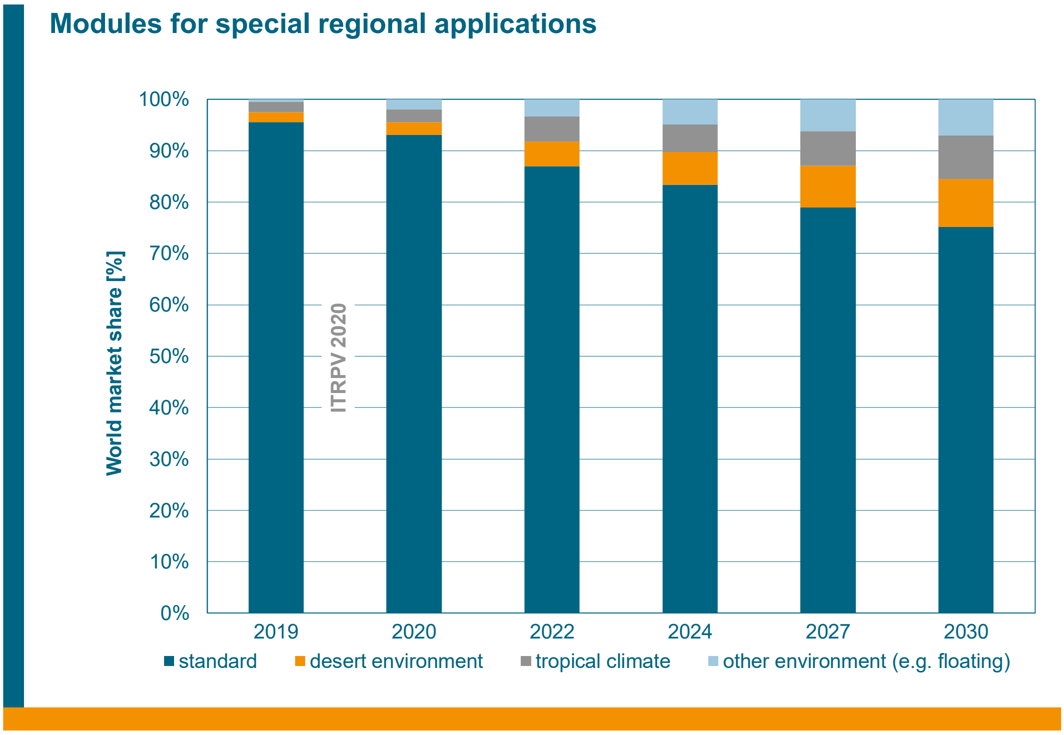


Fig. 65: Market share for special regional applications.

Another trend is the development of modules for special markets and environmental conditions. Fig. 65 shows the assumed market share of modules for special environmental conditions. It is still expected that the main market until 2030 will be for standard modules. Module for special environmental conditions like tropical climate, desert and floating PV applications will overall account about 25% over the next 10 years.

The junction box (J-box) is the electrical interface between the module and the system. We found that the internal electrical connection of the bypass diodes is and will be done mainly by soldering. Welding is gaining market share over the next years whereas clamping, the third technology, will be less used in the future. In addition, we see that the current single junction box concept as today's mainstream will be replaced by multiple junction box in the next years mainly due to the shift from full-cell module concepts to half-cell.

So-called smart J-box technologies are deployed to improve the power output of PV systems. Nevertheless, as shown in Fig. 66, the participants in our survey believe that standard J-box without any additional function except the bypass diodes will clearly dominate the market over the next 10 years.

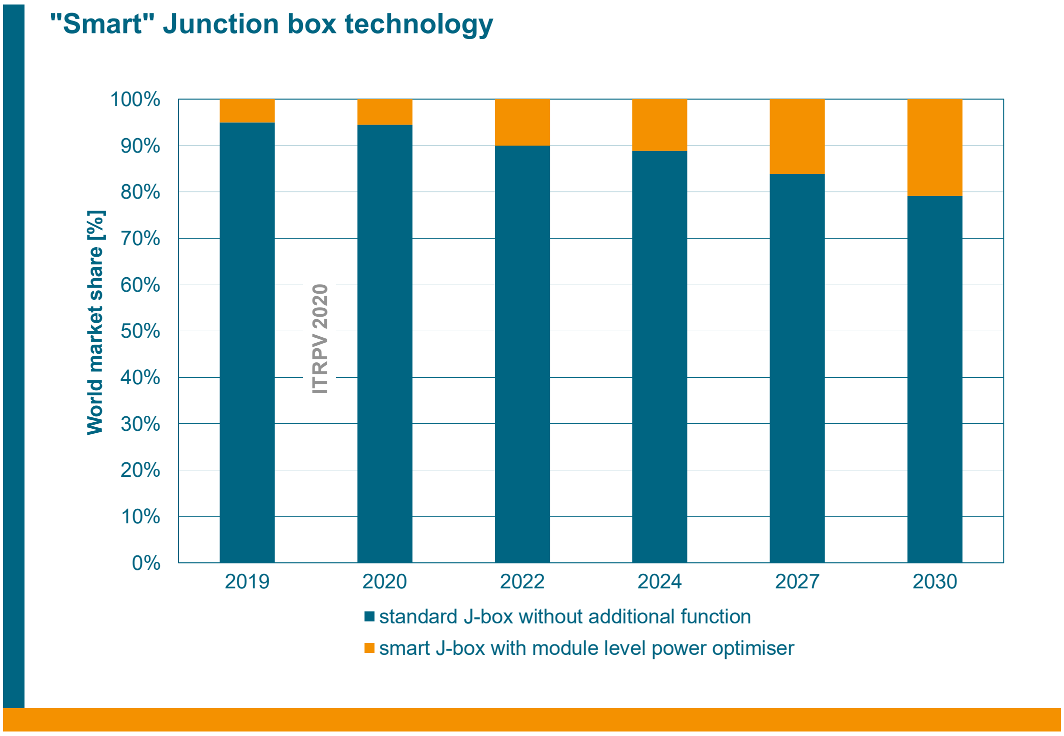


Fig. 66: Market trend for different J-box functionality - smart vs. standard J-box.

Fig. 67 shows the expected shares of module based microinverters. Integrated module mounted micro inverters will slightly increase the share from close to 10% in 2020 to about 23% within the next 10 years.

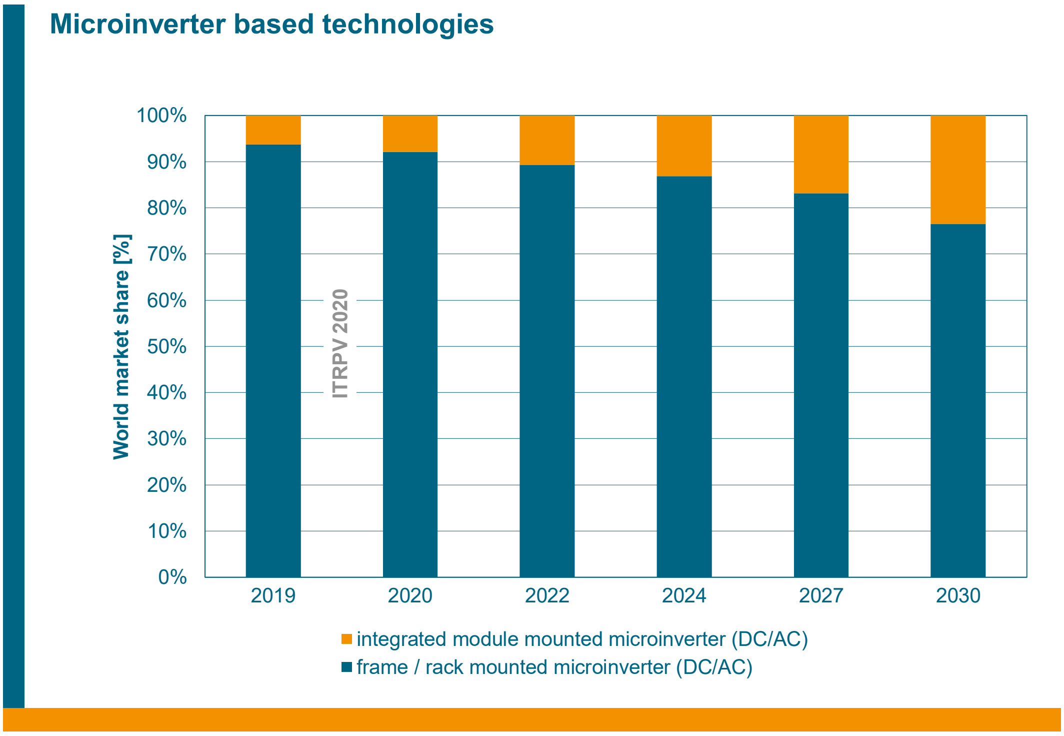


Fig. 67: Market trend for microinverter technologies.

The trend for J-box with special internal functions is shown in Fig. 68. Special features will be used in special markets. Standard junction boxes without additional functions will stay mainstream.

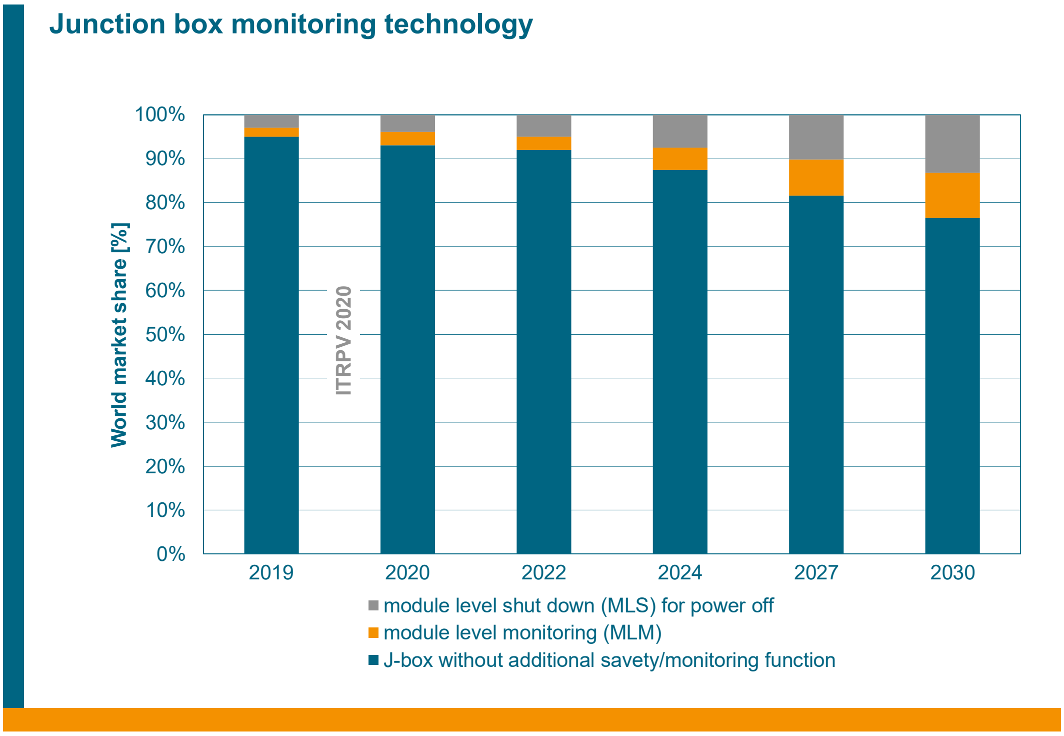


Fig. 68: Junction box monitoring technology.

Fig. 69 shows the estimated trend of warranty requirements and degradation parameters for the next years. The product warranty is expected to increase to 15 years and prospectively to 20 years in 2030. Performance warranty is expected to increase to 30 years from today 25 years. The degradation after the 1st year of operation will be reduced to 2%. This is mainly linked to the control of light induced degradation (LID) and to the light and elevated temperature induced degradation (LeTID). Understanding the degradation mechanisms and a tight control of the degradation are mandatory to ensure the warranty [17]. The implementation of gallium doped wafers as discussed in chapter 5.2.1 and shown in Fig. 8 will support this trend. Standards for LeTID testing are about to be developed [23]. Yearly degradation is expected to be reduced slightly from 0.7% today stepwise to 0.5% until 2022.

In order to maintain quality (for thinner cells as well), the solar cells used for module assembly should be free of micro-cracks. The contributing companies are considering testing all the products during the manufacturing process with EL inspection as standard and with a standardized procedure that has been in preparation [28].

The contributors consider Potential Induced Degradation (PID)-resistant cell and module concepts also as market standard.

Higher level of stress testing for PID is still common. Many test labs apply test conditions beyond the minimum levels described in IEC TS 62804. Currently IEC TC82 is working on a next edition of IEC 61215 which will include testing for PID. At the same time, there has been no industry-wide accepted and applied definition of micro-cracks.

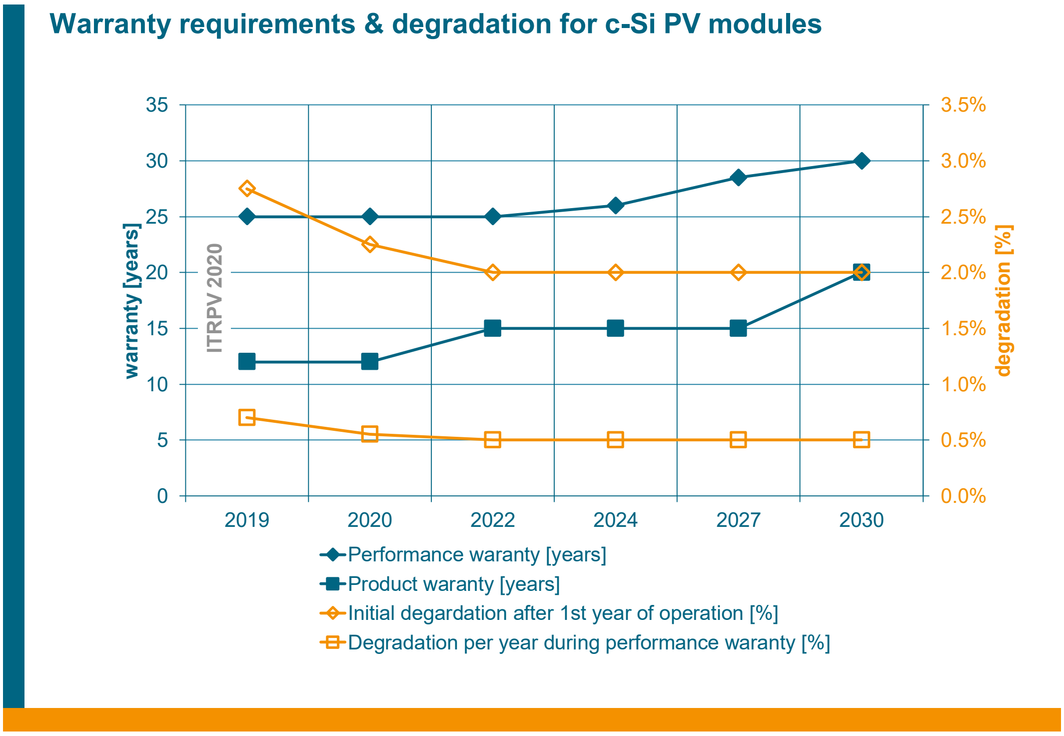


Fig. 69:Expected trend for product warranties and degradation of c-Si modules.

8. Smart Fab Status

Using the tools in an efficient way is mandatory to keep path with required cost reductions. Fig. 70 summarizes the status of Overall Equipment Efficiency (OEE) according to SEMI E10 [29] in state-of-the-art cell production facilities. Current values around 90% for back end and thermal must be increased during the next years.

OEE Improvements will mainly be realized by improving tool and fab automation, automatic recipe downloads, via integration of the tools into Manufacturing Execution Systems (MES) and automatic dispatching systems as well as automated wafer-to-wafer and lot-to-lot process control systems. In addition, yield improvements for all tools have to be assured despite the introduction of larger and thinner wafer.

Fig. 71 shows the status and the trend regarding machine learning and automation. Automation fab logistic systems are widely present in today's fabs and will be standard in the future. Machine learning to optimize the logistic system is in use in today's state of the art fabs and will be standard after 2025 together with automated process control systems.

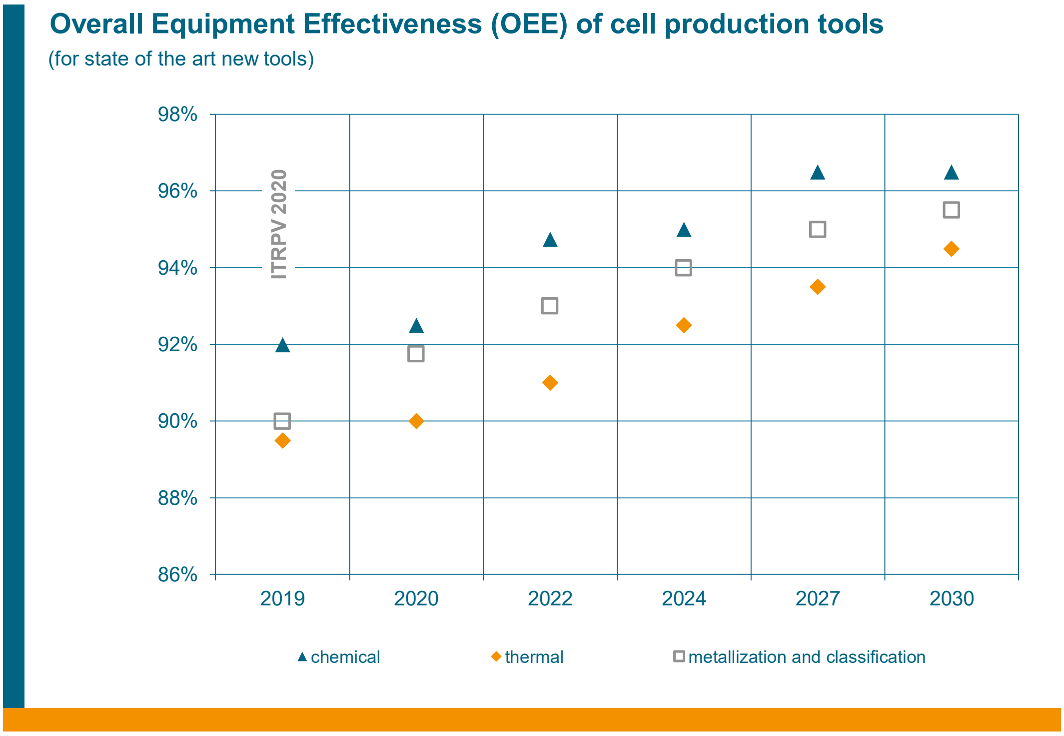


Fig. 70: OEE trend of state of the art new cell tools in new production facilities.

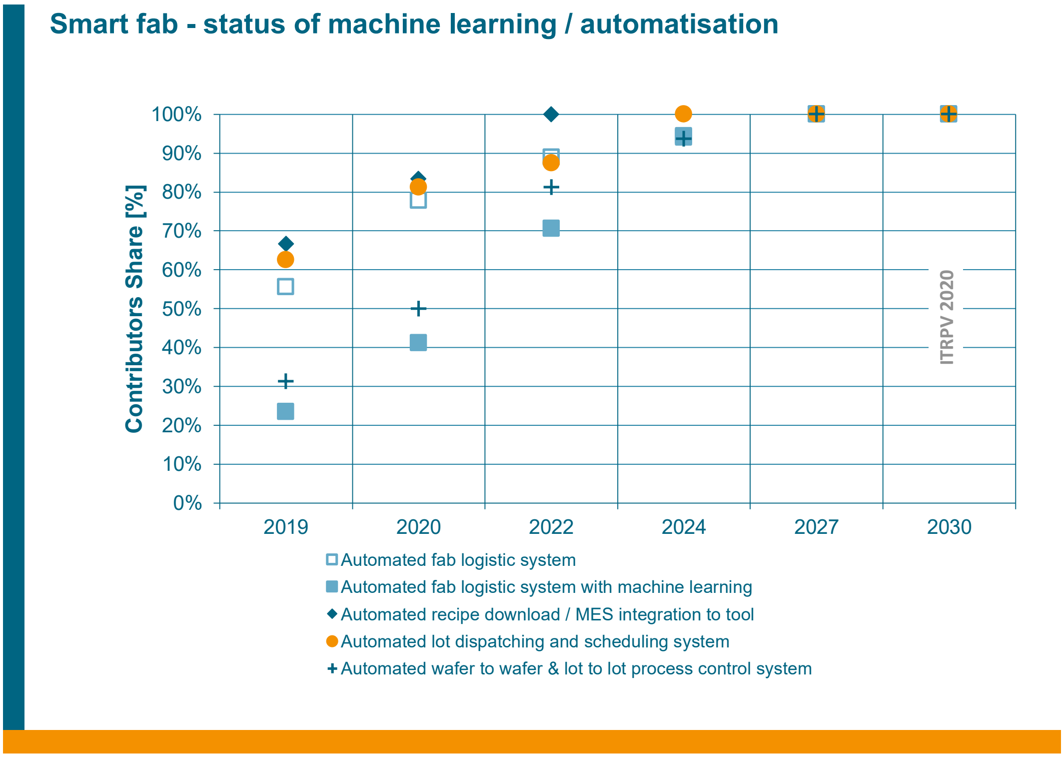


Fig. 71: Machine learning status and implementation of MES outlook for new cell fabs.

The expected trend of measures regarding production tracking, essential for the automation of fab logistics is shown in Fig. 72. It must be emphasized that the tracking from cell to module manufacturing will increase to 100% within the next years.

Status of WIP tracking

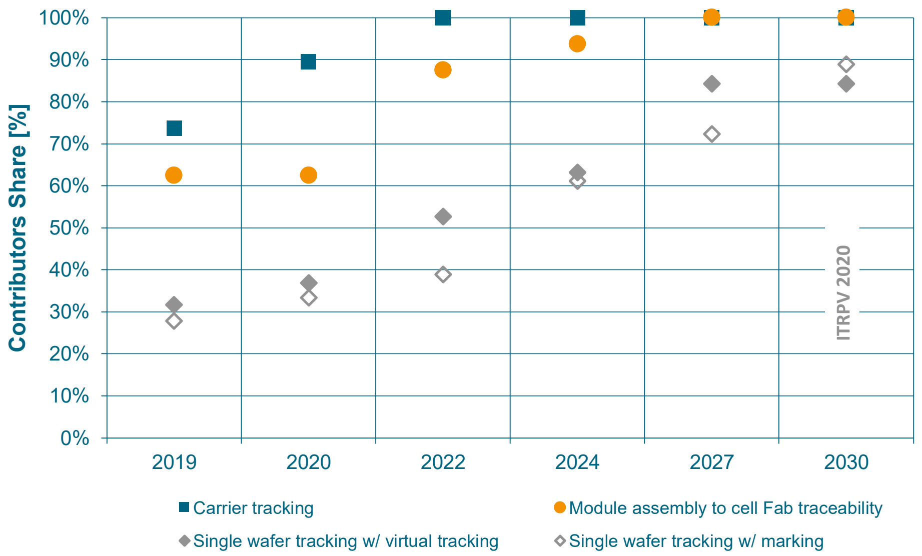


Fig. 72: Status and trend of WIP tracking methods in state of the art cell and module production lines.

Inline process control

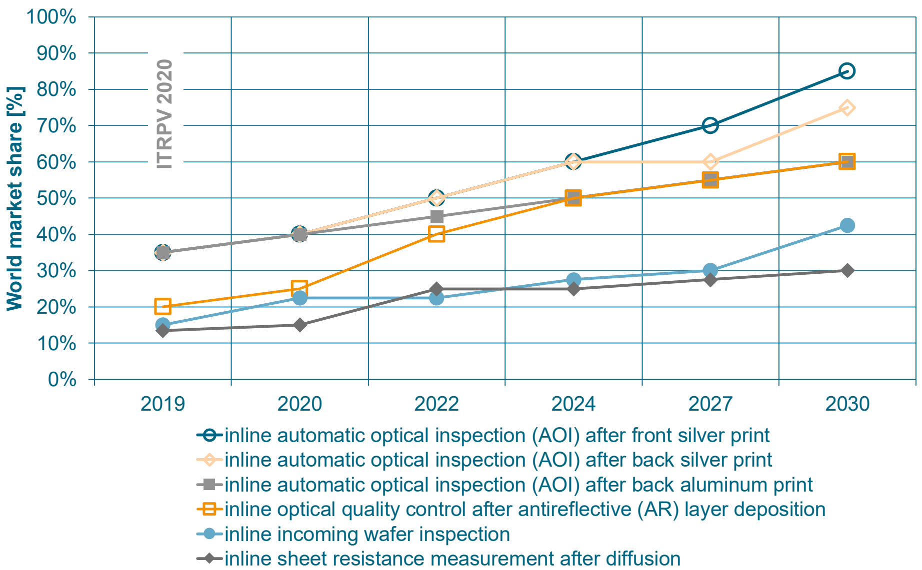


Fig. 73: Market share of inline process control for incoming wafer quality, sheet resistance, antireflective layer deposition, and for printing quality at rear and front side printing.

Inline process control in cell and module production lines becomes more and more important to ensure high production yields and high average efficiencies with tight distributions, perfect optical appearance, and longtime product reliability.

Fig. 73 and Fig. 74 summarize the assumptions about inline process control of selected cell process parameters.

Fig. 73 shows that cell appearance and cell back-end process inspections are more automated than the front-end processes. Automatic inspection (AI) of incoming wafer is assumed to be in use in 2020 for about 20% of all cell production lines. Sorting out of spec material is important to ensure high cell production yields. Nevertheless, incoming inspection is mainly deployed on sampling base. Measurement systems for sheet resistance are implemented in contemporary production lines for diffusion process monitoring in 2022 for only about 20% of the production lines and up to 30% in 2030. The control of the front side antireflective (AR) layer is in use at about 10% of production lines today. Nevertheless, the penetration in 2030 is expected to reach 60%. Automatic optical inspection (AOI) in print inspection is most widely used today with about 40% of the lines in 2020 and is expected to be implemented in up to 80% of all lines by 2030 especially for the front side printing.

Fig. 74 shows that AI is widely used in cell test and sorting. AOI including front side color inspection at cell test is standard in new cell production lines. It is expected that in 2022 about 90% of all lines will be equipped with AOI for front and rear side inspection. The trend is clear to be close to 100% in 2030.

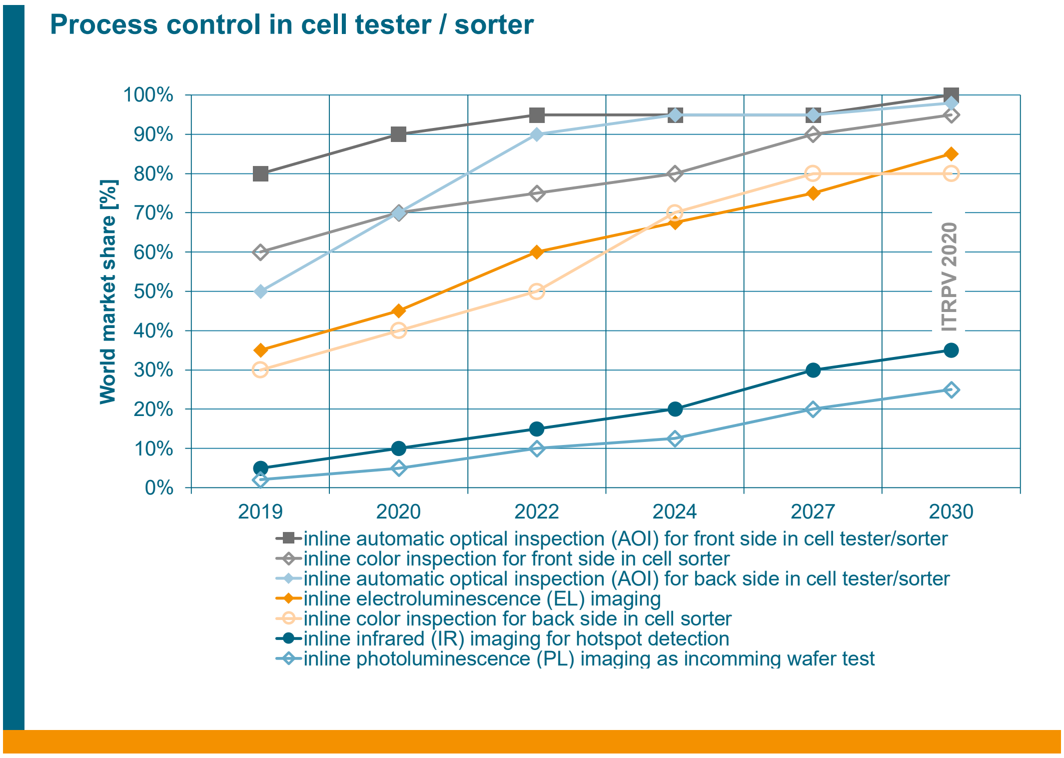


Fig. 74: Market share of different inline Automated Inspection (AI) systems for process control at cell test.

In addition, we see an increasing share of rear side color inspection for bifacial cells and increasing deployment of EL, IR, and PL imaging systems. The latter two are considered to have the lowest implementation share with ≤ 10% in 2020 and in only about 30% of all production lines in 2030.

The trends for inline testing and manufacturing execution systems (MES) in module production lines are summarized in Fig. 75. EL inspection of modules is standard with 90% market share in 2020 and 100% after 2023. A similar trend is visible in AOI of cells in the stringer process. IR and cell color inspection in the stringer in module production are expected stay on low levels as those inspections are already done at cell test. AOI after lamination will also not exceed 30% in the future.

The implementation of MES progresses - 2020 share of 45% will increase systematically to 80% in 2030. This is a clear sign towards further automation and smart manufacturing in c-Si module production.

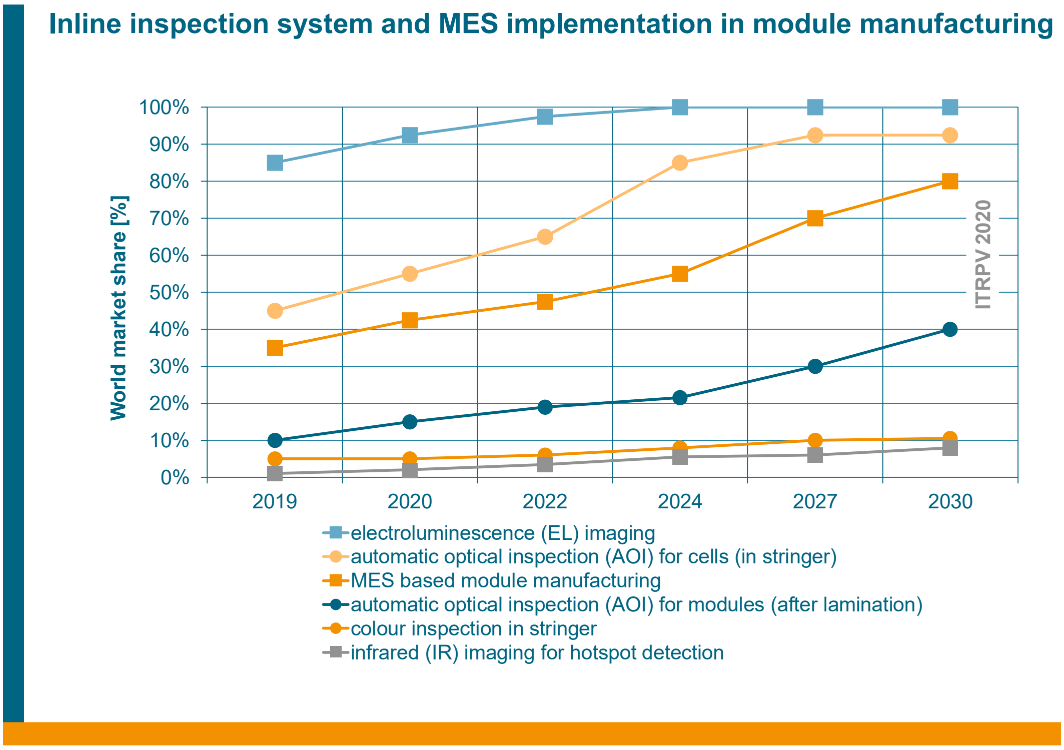


Fig. 75: Trends of inline inspection systems and MES implementation in module production lines.

9. Results of 2019 | System

9.1.Components

Due to the significant reduction of PV module prices over the last few years, balance of system (BOS) costs have become a crucial factor in overall system costs and thus the levelized cost of electricity (LCOE) as well. Besides warranties for the product and the product performance as well as the degradation of the modules during the operation lifetime an increase in system voltage and the trend to install more 1-axis tracking systems are important parameters to reduce LCOE.

In Fig. 76 the relative developments of system costs and of system cost elements for large systems > 100 kWp are shown. We considered the average trend for systems in three regions: Europe, Asia, and the US. The module will stay the most expensive single cost element in a PV system. A cost reduction by about 40% is expected within the next 10 years due to ongoing module price learning. The module share is expected to decrease only slightly from about 41% in 2020 to about 36% in 2030.

One trend to be expected on system level is the trend toward an increase of system voltage from 1,000 V to 1,500 V - from 2021 onwards the market for 1,500 V systems will be > 50%, attaining a market share of > 75% after 2024 onwards (see Fig. 77). The increase in system voltage represents an important measure for lowering resistive losses and BOS costs by reducing the required diameter of the connection cables within a PV system.

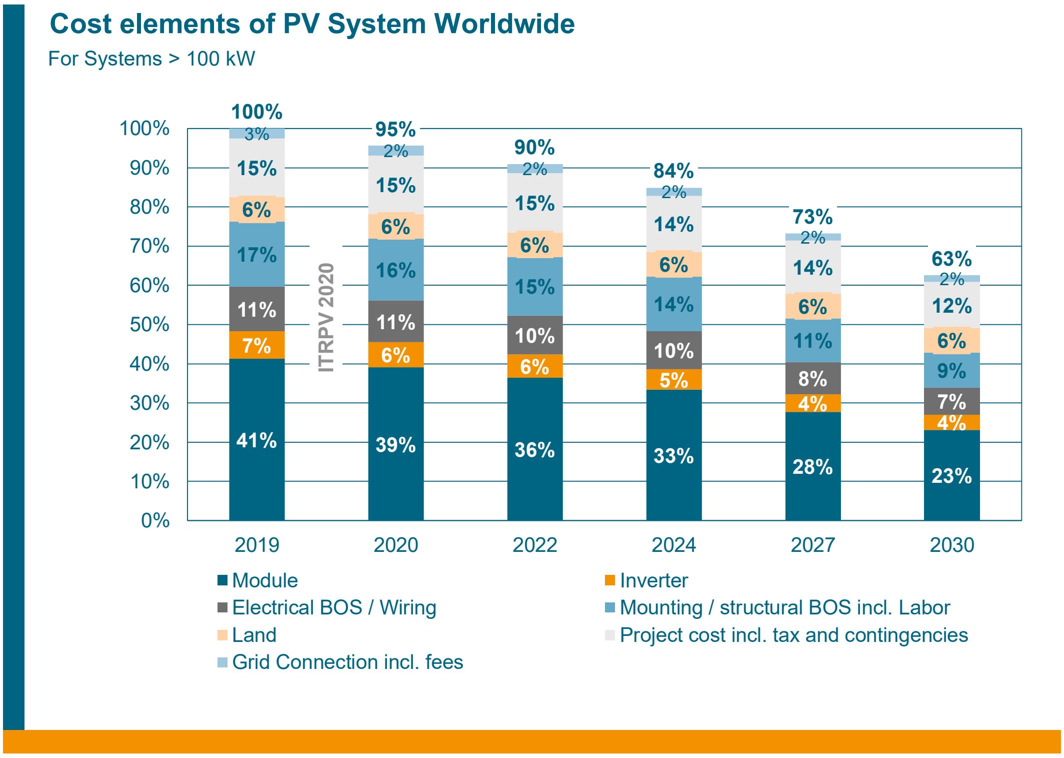


Fig. 76: Relative system cost development for systems > 100 kW Worldwide (2019 = 100%).

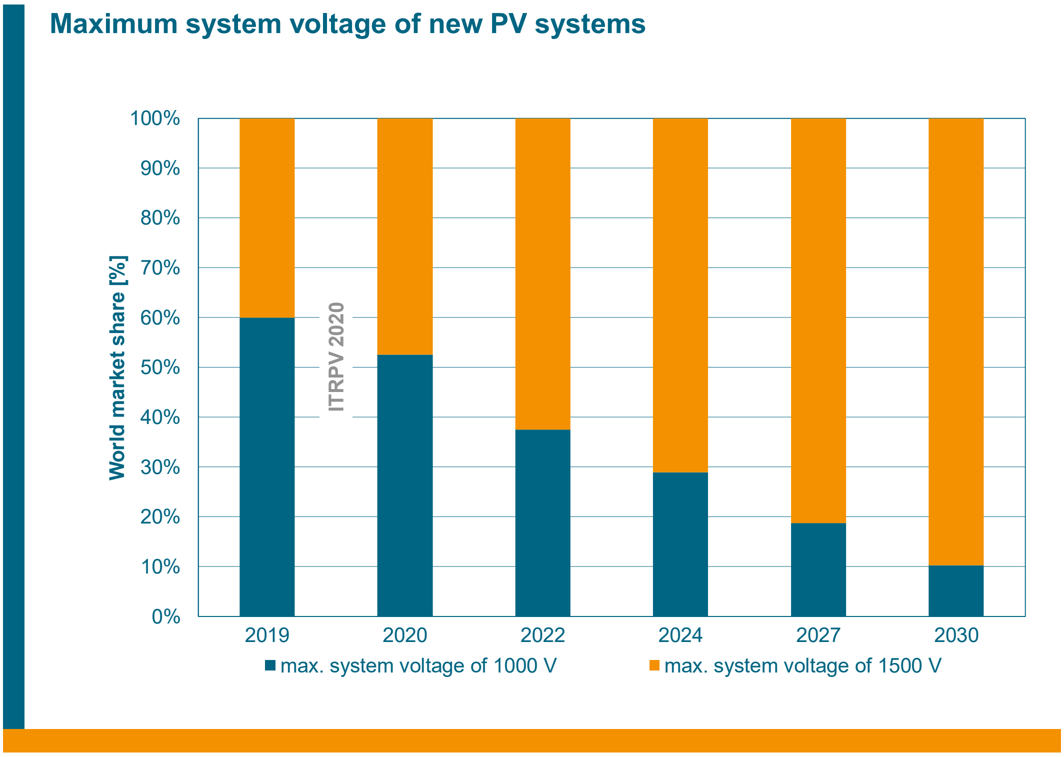


Fig. 77: Trend of maximum system voltage for systems > 100kW.

Another long-term trend on system level is tracking system deployment in order to maximize the energy output of PV systems. The market share of tracking systems in large scale c-Si based PV systems is shown in Fig. 78.

Fixed tilt installation will stay mainstream, 1-axis tracking systems will increase market share from ≈30% in 2020 to ≈40% in 2030. 2-axis tracking will remain negligible for c-Si technology with a constant market share of around 1% during the next decade.

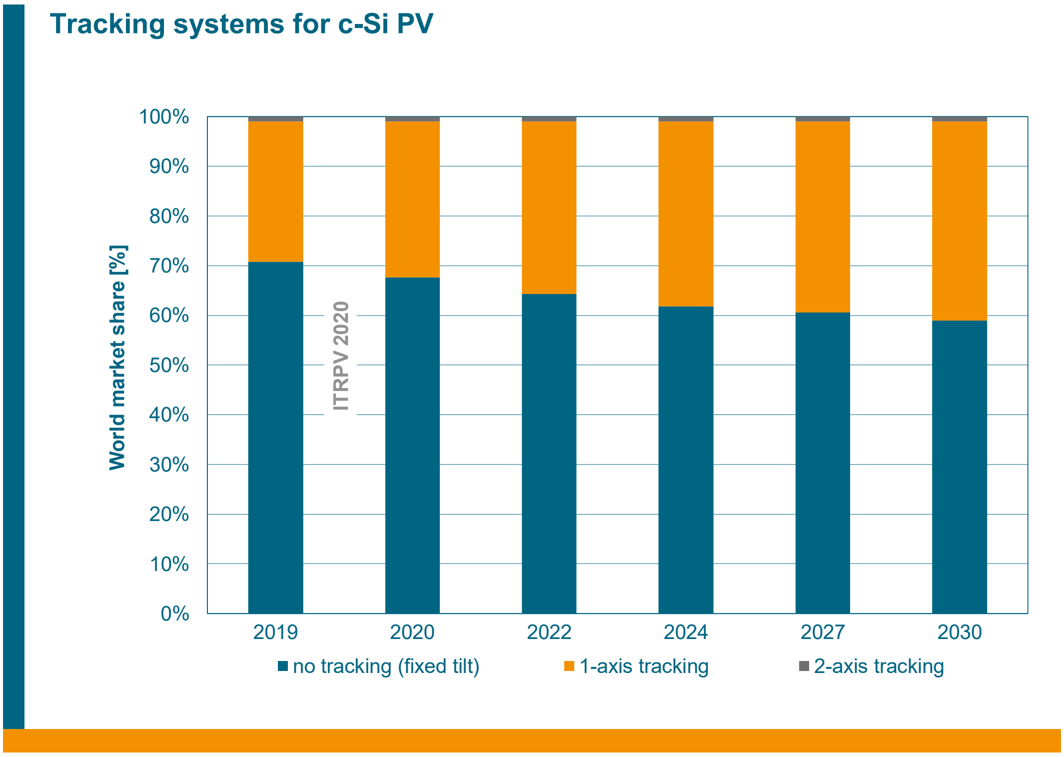


Fig. 78: Market share of tracking systems for c-Si PV installations.

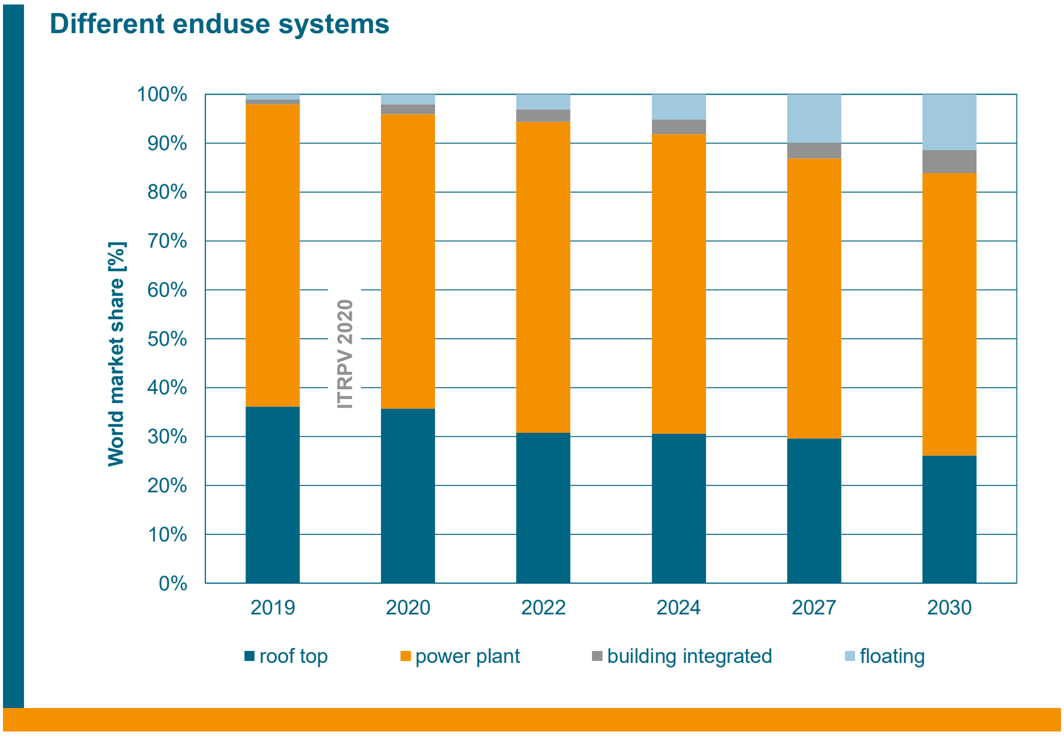


Fig. 79: Share of PV system applications in enduser markets.

Fig. 79 shows the trend for different system installations. Ground based power plants will dominate the market accounting for about 60% of all installations. The fraction of roof top systems will decrease slightly within the next decade. Floating PV systems will increase the market share to about 10%. Building integrated PV is expected not to exceed 5% until 2030.

More of PV installations will be combined with storage systems - Fig. 80 shows that the share will increase from 4% in 2020 to 50% in 2030.

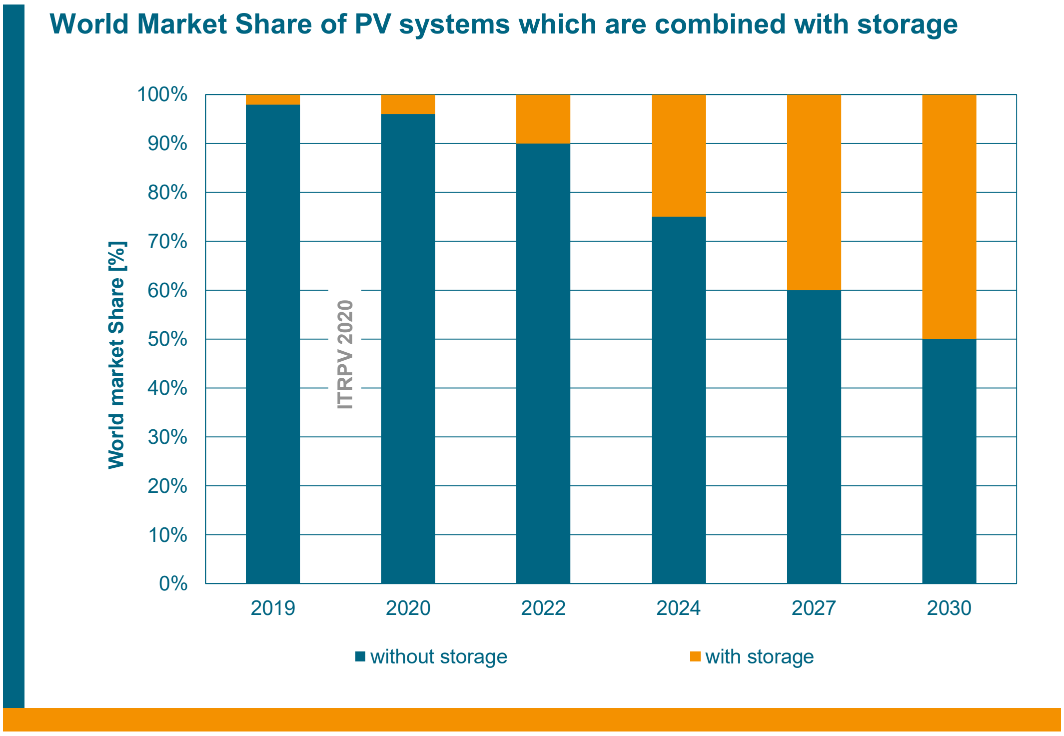


Fig. 80: Market share of PV systems combined with or without storage.

9.2. LCOE

The levelized cost of electricity (LCOE) is a commonly recognized economic metric for comparing the relative costs of different renewable and non-renewable electricity generation technologies. Along with the system capital cost and the insolation level, LCOE is also strongly dependent upon operations and maintenance (O&M) expenses, the project financing structure and the expected rates of return for debt and equity stakeholders, national and local incentives, and the usable service life of the system. We have used NREL's System Advisor Model (SAM) to calculate 2019 benchmark and future scenarios of PV LCOE for large PV systems deployed in different insolation conditions (see Fig. 81) [30, 31, 32].

Our survey results reflect that the underlying system capital cost drivers are strongly dependent upon location. We have calculated a global average of 720 US$/kW(DC) capital cost for utility-scale systems in 2019. The so-called 'soft costs' including project developer overhead and profit, sales tax, and permitting fees could add around another 150-300 US$/kW(DC) for large-scale systems in the U.S. and Europe in 2019. These items typically have the greatest variance across the globe and from project-to-project; therefore, they are not included in the ITRPV. The system cost trends depicted in Fig. 81 assume that total direct utility-scale capital costs will decline to around 420 US$/kW(DC) in 2030.

As can be seen in Fig. 81, LCOE values between 0.025 and 0.061 US$ are calculated to be feasible today across the range of solar insolation levels. Improvements in product reliability and energy yield, increases in system voltages and better power electronics, and increased use of 1-axis tracking systems are noteworthy opportunities to reduce LCOE. Considering the system capital trends anticipated by the ITRPV, PV LCOE in the range of 0.02 to 0.04 US$ are predicted by the year 2030. Due to the significant reduction of capital costs over the past decade, operations, and maintenance (O&M) expenses have become proportionally more significant factors behind the 2019 benchmark and projected LCOE of PV systems.

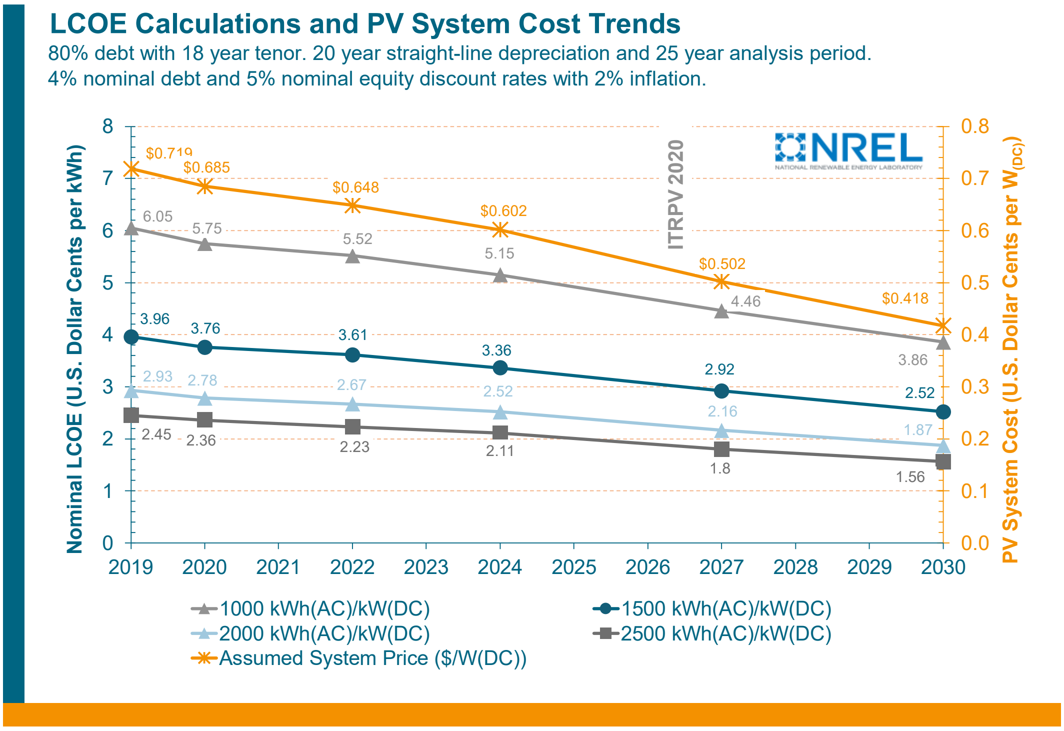


Fig. 81: Calculated global avarage capital cost for utility scale systems and calculated LCOE values for different insolation conditions. Financial conditions: 80% debt, 18-year loan tenor, 20-year straight line depreciation and 25 years usable system service life. 4%/a nominal debt rate, 5%/a nominal equity discount rate, 2%/a inflation rate. The calculations were performed using NREL's System Advisor Model (SAM)[30].

For our calculations we have assumed 25 years of usable system service life; however, it is expected that advances in module and BOS technology as outlined in the ITRPV could enable an extension of the system service life to 30 years (see Fig. 69) or maybe even more. Advances in system life would make it possible to reduce LCOE levels even further. Lower financing rates due to PV becoming a lower risk electrical energy generation technology may also allow the 2030 LCOE levels to be reached earlier. This will make PV power generation a more cost-competitive and valuable contributor to the world's future energy mix, as discussed in the next section.

10. Outlook

10.1. PV learning curve

Chapter 3 reviews the learning curve status. Fig. 1 shows the price learning curve and the calculated price learning rate. The current learning rate is calculated to 23.5% using all historic price data points from 1979 to 2019. However, considering only the data points from 2006 onward, the learning rate raises to 40% as shown in Fig. 82.

2006 was the last year of a longer period of silicon shortage. It marks the beginning of c-Si PV mass production in China and thereby the entry into a period of continuous capacity extensions after the scarcity situation of silicon and PV modules during the period between 2004 and 2006.

Learning curve for module price as a function of cumulative shipments

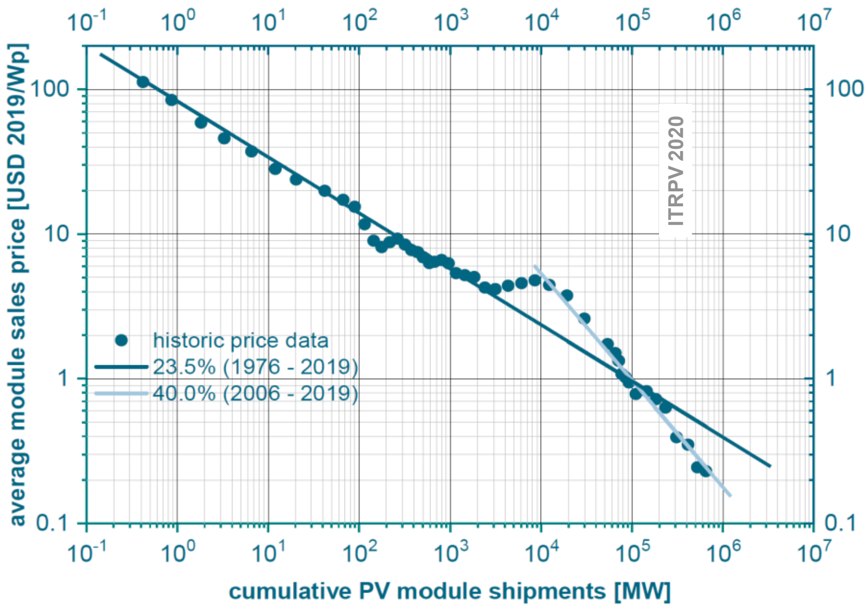


Fig. 82: Learning curve of module spot market price as a function of cumulative PV module shipments and calculated learning rates for the period 1979 to 2019 and 2006 to 2019, respectively.

Based on the findings in the ITRPV we started in the 8th edition the analysis about the breakdown to the two basic learning contributors - module power learning and reduction of price (cost) per piece learning.

Tab. 2 summarizes average module efficiencies at different years. The price values were taken from the learning curve while module efficiencies were assumed as average module powers of p-type mc-Si and mono-Si modules of ITRPV reports (3rd to 11th edition) the module efficiency of 1980 was found in [33]. A quite standardized module size of about 1.64 m² was used as base for module efficiency calculations until 2018.

The switch to larger wafer formats as shown in Fig. 15 and Fig. 16 resulted in a variety of new module formats. The 2019 mainstream module format uses 60 full-cells / 120 half-cells (see Fig. 63). The corresponding averaged module area increased from 1.64 m² to about 1.7 m² [34]. Calculated average module power is 326 Wp. Based on these facts, we found an average module efficiency of 19.2% for 2019. Module efficiency more than doubled compared to 1980 and increased by 30% compared to 2010.

Tab. 2: Yearly learning for module efficiency and price per piece based on module price data (2010 = 100%) [5, 6, 7], module efficiencies calculated from ITRPV module power values (3rd to 10th edition) and [34]; 1980 module power is calculated from efficiency in [33].

Year over year learning

Year	1980	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019
avg. Module power p- type (ITRPV-data)	147.6	241.5	248	253	262	267.5	278.5	287.5	290	302.5	326
Module efficency 60 cell [%], avg. Mod. area: 1.64m² [5], 2019: 1.7m²	9	14.7	15.1	15.4	16	16.3	17	17.5	17.7	18.4	19.2
Module price [$2019]	37.23	1.74	1.08	0.78	0.82	0.72	0.63	0.39	0.35	0.24	0.23
relative module price reduction [%]		95.34	37.77	27.37	-4.35	11.81	12.42	37.65	11.08	30.27	5.86
Module price (Wp-increase only) [$2019/Wp]		1.74	1.69	1.66	1.59	1.56	1.50	1.46	1.44	1.38	1.33
Module price (cost reduction per piece only) [$2019/Wp]		1.74	1.13	0.86	0.96	0.89	0.87	0.672	0.64	0.60	0.64

Learning curve for module price as a function of cumulative shipments

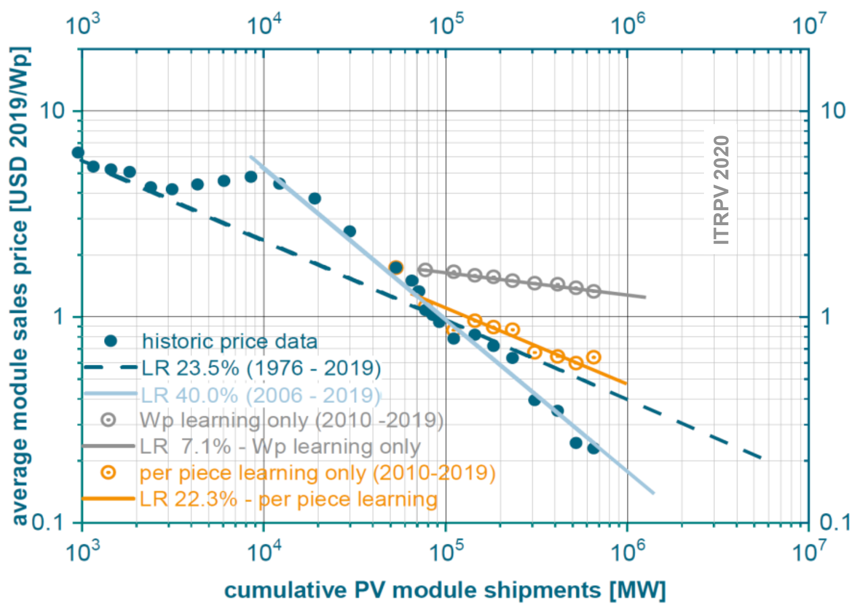


Fig. 83: Log-log plot learning curve of module spot market price as a function of cumulative PV module shipments; update on calculated learning rates for the period 1976 to 2019 and 2006 to 2019 respectively, calculated rates for Wp learning and per piece learning according to Tab. 2.

Fig. 83 shows the plot of Tab. 2 data points for Wp learning and per piece learning, respectively. The calculated corresponding learning rates of 7.1% for Wp learning and 22.3% for per piece learning indicate that the main contribution of the price learning arose from per piece reductions. This is in line with the findings in [4] and emphasizes again that only the combination of Wp learning and cost reduction grants the resulting learning despite per piece learning in 2019 was not in line with former years, mainly due to the introduction of the larger module formats. The price stabilization resulted in a positive stabilization of operating margins for solar companies [32]. Fig. 84 shows the data of Fig. 83 in a linear plot.

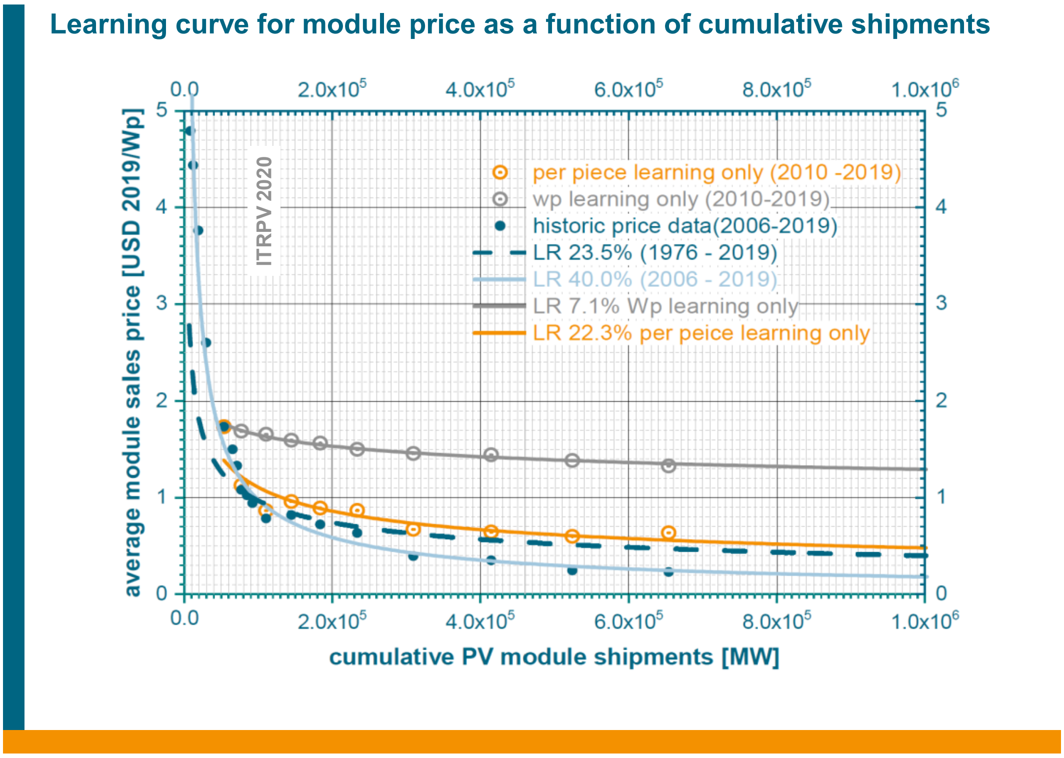


Fig. 84: Linear plot of Fig. 83.

10.2. PV market development considerations

PV will play a key role in a future net zero greenhouse gas emission energy system that has to be installed until 2050 [35]. The most widely publicly discussed PV-related topics and trends are about installed PV module power (DC), module shipments, as well as about PV generated electricity scenarios.

A look at the supplier side, to follow the market development of PV modules, cells, wafers and polysilicon, is less spectacular, but it is essential for investment planning.

The analysis of the annual PV market development until 2050 was started in the ITRPV 6th edition. In this 11th edition we discuss the analysis of the global energy system based on 100% renewable energy - already found in the ITRPV 10th edition [36], results of a study about future PV module price development [37], and a 2019 energy outlook scenario [38] with a view to 2019 PV shipments.

We consider four scenarios; scenarios 1, 3, and 4 are superimposing calculated results for different world regions:

1. Low scenario: (power sector) — 7.6 TWp installed PV in 2050, generating 9.3 PWh ≈22% of global electricity according to BNEF NEO 2019 [38].

2. Medium scenario: (all sectors) — 19.8 TWp installed PV in 2050, generating 31 PWh ≈20% of global primary energy demand according to [37].

3. Electricity scenario: (power sector) — 22.0 TWp installed PV in 2050, generating 38 PWh ≈69% of global electricity [35].

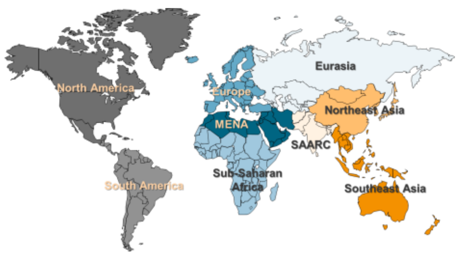
4. Broad electrification: (all sectors) — 63.4 TWp installed PV in 2050, generating 104 PWh ≈69% of global primary energy demand (including power & heat, transport, and desalination) [36].

Details of the scenarios and the corresponding considered regions are summarized in Tab. 3. Fig. 85 - Fig. 88 display these scenarios showing the calculated cumulated PV installation in 5-year steps, the corresponding 5-year average annual PV market without and with replacement after 25 years, and the historic annual shipments according to Fig. 1.

Tab. 3: Summary of regional results for the different scenarios.

Summary of regional results for the different scenarios

Scenario	Region	Installed power 2050 [TWp]	PV Power generation 2050 [PWh]
Low scenario	Americas	1.3	
	AsiaPacific	3.4	
	ROW	0.4	
	EMEA	2.5	
	total	7.6	9.3
Medium scenario	total	22.0	31.0
Electricity scenario	Sub-Saharan Africa	1.3	
	MENA	1.4	
	North America	2.5	
	Northeast Asia	7.4	
	SAARC	3.7	
	South America	0.8	
	Southeast Asia	2.4	
	Eurasia	0.4	
	Europe	2.0	
	total	22.0	38.1
100% Renewables	Sub-Saharan Africa	2.9	
	MENA	4.6	
	North America	7.0	
	Northeast Asia	17.8	
	SAARC	11.9	
	South America	2.3	
	Southeast Asia	5.3	
	Eurasia	2.6	
	Europe	8.9	
	total	63.4	104.0



ITRPV 2020

Fig. 85 illustrates scenario 1 - PV based power generation figures, published in the Bloomberg NEO 2019, a current analysis about electrical power generation and consumption until 2050, based on assumptions about population growth and energy consumption trends [38]. It considers the limitation of global temperature increase to 2°C at the end of the 21st century. This scenario assumes a PV installation of about 7.6 TWp being enough to cover 22% of global electricity demand in 2050. Energy yield in this scenario is assumed to be about 1.2 kWh/kWp. The maximum addressable market including replacements after 25 years is calculated to 400 GWp in 2050.
NEO 2019 assumes that PV market is growing until 2020 not above 110 GW/year. Historic shipments plotted in Fig. 85 are above the assumed addressable market of this scenario. NEO 2019 is underestimating the market potential of PV installations from our point of view.

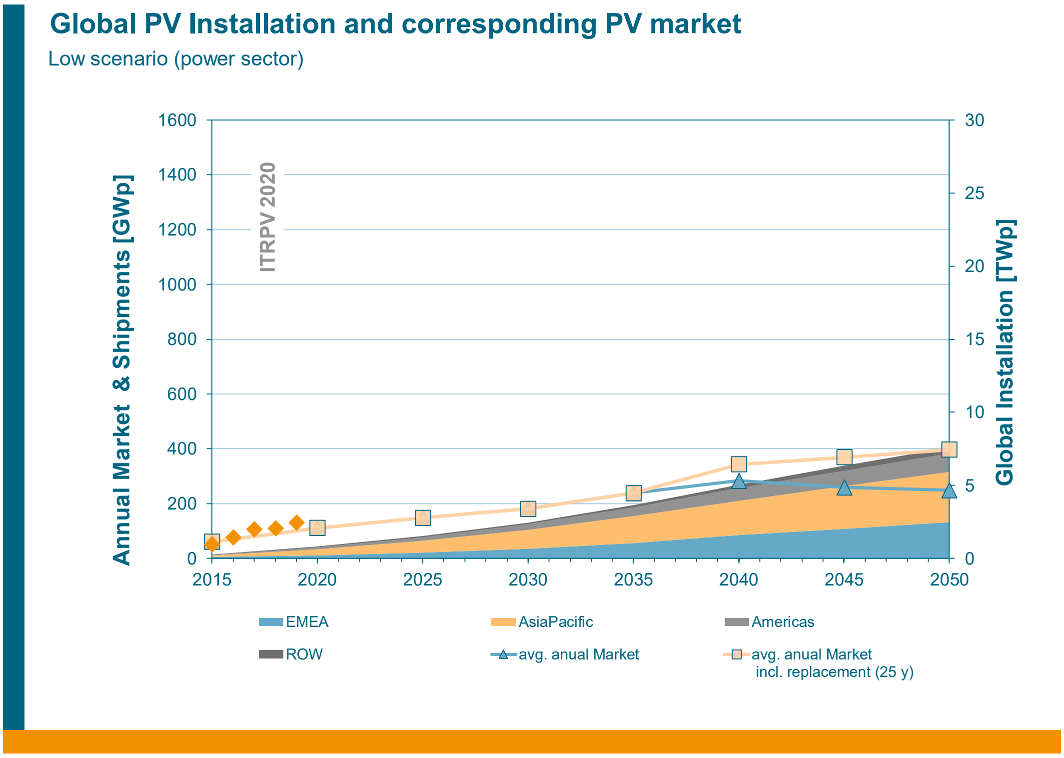


Fig. 85: Scenario 1: Cumulative installed PV module power and 5-year average annual market according to Scenario 1, NEO 2019 assuming 7.6 TWp installed PV module power in 2050 [38].

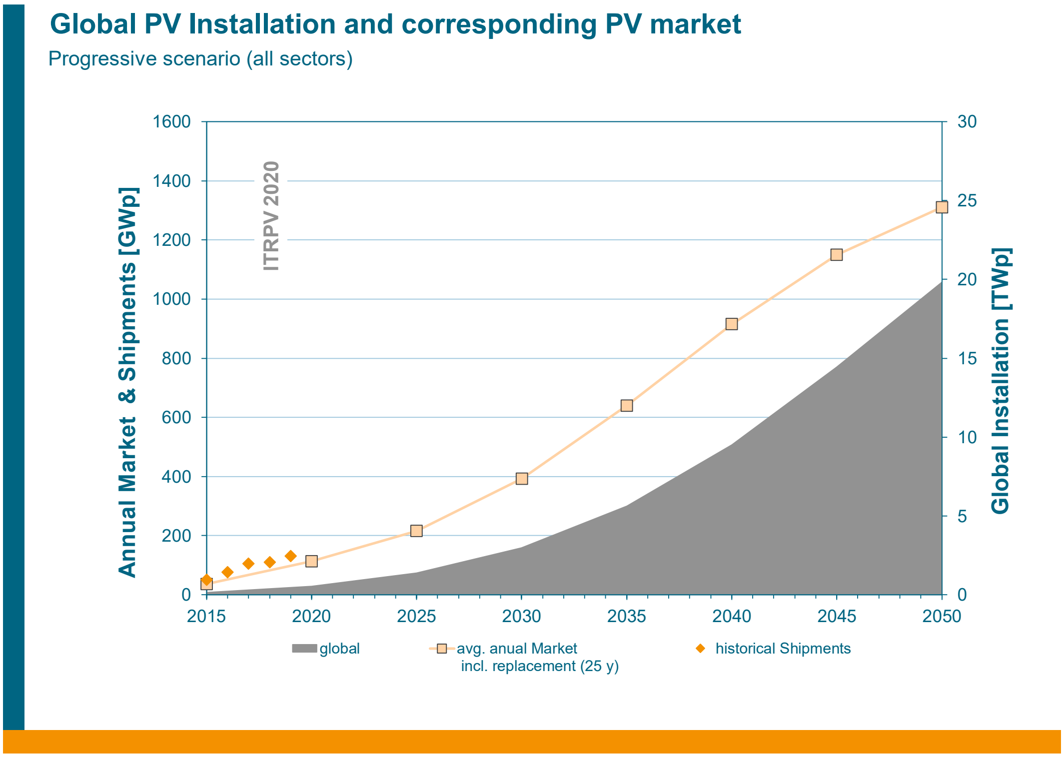


Fig. 86: Scenario 2: annual PV market and corresponding cummulated global installation of 19.8 TWp installed PV in 2050 including replacements after 25 years, acording to [37].

Scenario 2 is shown in Fig. 86. In this scenario 19.8 TWp of installed PV modules in 2050 are calculated for. Energy yield in this scenario is assumed to be 1.6 kWh/kWp.

Hoffmann and Metz are calculating in [37] the annual PV market size/production volume (PV_a) with a logistic growth approach in order to find the market volume point for a module ex-works and whole-sale price of 10 US$ct/Wp.

$$PV_a(t) = 1.5\,TWp/((1 + exp(0.15 * (2035 - t)))$$

According to [37], a module whole sales price of 10 US$ct/Wp will be reached at a cumulated volume of about 10 TWp - at 2040 or so as shown in Fig. 86. Despite our opinion that the market requirement will determine the production volume and not vice versa, we consider the analysis of Hoffmann and Metz as an excellent confirmation of the competitiveness of PV.

Scenario 3 and 4 consider the need of a net zero greenhouse gas emission energy system no later than 2050. PV is the key technology to reach a 100% renewable energy and greenhouse gas emission free energy economy by 2050, considering the three main energy consumption field of power & heat, transportation, and desalination for 9 major global regions as summarized in Tab. 3, a model pre-sented in [36] and [39] is used.

The Electricity scenario shown in Fig. 87 considers the contribution of PV in a 100% renewable energy-based power sector [35]. The 22.0 TWp will generate approximately 38.1 PWh in 2050.

Fig. 88 shows the required PV installation trend to reach the Broad electrification scenario 4. This will be the path towards a zero-greenhouse gas emission economy in 2050.

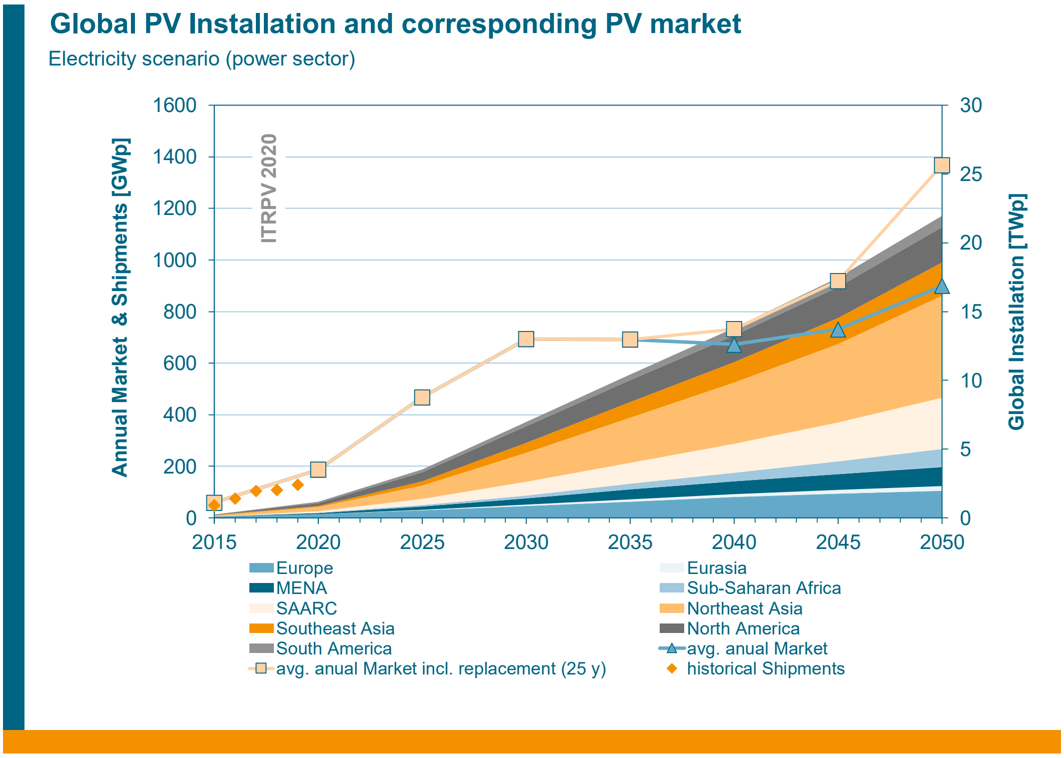


Fig. 87: Scenario 3: Cumulative installed PV module power and 5-year average annual market for global PV module installation of 22.0 TWp in 2050 (see Tab. 3 and [35]).

Scenario 3 and 4 consider an average system energy yield of approximately 1730 kWh/kWp and 1650 kWh/kWp respectively realized by power plant installations in higher insolation regions, also taking single-axis tracking with higher yields into account.

It is remarkable that the historic shipments are nearly in line with the required shipments in scenario 4 and slightly below scenario 3, respectively.

All four scenarios show that there will be a considerable module market in the future. Latest announcements predict that the installation of huge production capacities will continue and emphasize that higher growth scenarios will be controllable [40]. Nevertheless, there is a risk of overheated market present especially as production capacity is currently exceeding the shipments by about 80% as discussed in chapter 1. High PV module demand will be fuelled by the fact that PV electricity will become the cheapest source of electricity globally. Cheap PV electricity will drive power-to-X demand so that other energy sectors can also benefit from low cost PV. Scenario 4 assumes a broad electrification for fulfilling the targets of the Paris Agreement for a least cost energy system.
The scenario 1 will be no challenge at all for the PV industry. Production capacities of up to 1TWp as discussed in Scenario 2 and 3 seem to be manageable even with the today's mainstream technologies. Production capacities beyond 1 TWp appear more challenging.

Beside the expected increase of PV installation and production, recycling needs will become more important in the future - as business opportunity and as challenge [41].

Progressive tool concepts in cell manufacturing for production lines with matched throughput between front and backend, as discussed in chapter 6.2, will support future production capacity increase. Anyhow, a further increase of production beyond the 1 TWp level will require further improved production technologies.

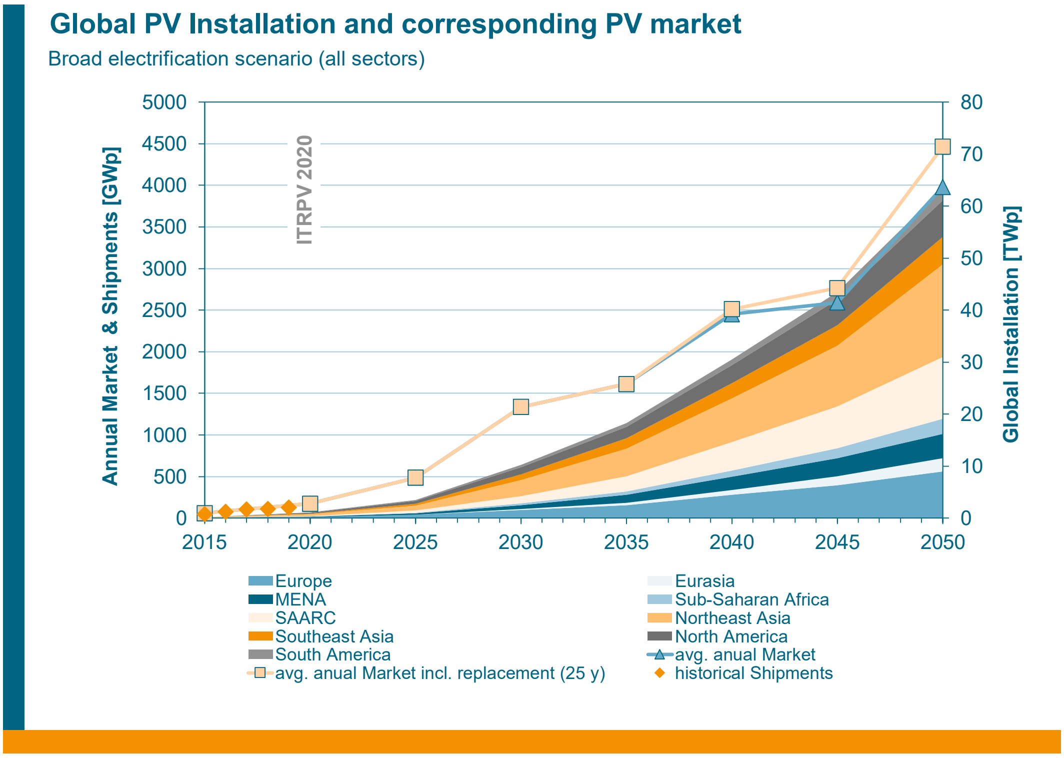


Fig. 88: Scenario 4: Cumulative installed PV module power and 5-year average annual market for global PV module installation of 63.4 TWp in 2050 in a zero greenhouse gas emission economy - broad electrification (see Tab. 3 and [39]).

PV equipment suppliers have to support upgrades of existing production capacities to larger wafer formats, the continued upgrades to PERC and the installation of new production capacities capable for M6 wafer formats and beyond. New c-Si capacities for cell and module will be implemented for the mature PERC concepts and for upcoming n-type cell technologies - right from the beginning capable for larger wafer formats as discussed in chapter 5.3.

The continued support of depreciated production lines, the replacement of worn-out equipment and the support of upcoming capacity expansions with smart factory approaches as discussed in chapter 8. will constitute considerable business segments in the future. All these facts emphasize the positive outlook for the whole c-Si PV industry.

All activities for increasing module power and cell efficiency, ensuring more efficient poly-Si usage, and supporting a higher utilization of production capacities as discussed in the current ITRPV edition will help manufacturers in their efforts to supply the market with highly competitive and reliable c-Si PV power generation products in the years to come. The price learning of PV modules will continue, and this will push the LCOE reduction of PV systems.

10.3. Accuracy of roadmap projections

The ITRPV has been publishing reports since 2010. Since the 1st edition, the investigated parameters have been reported as median values of the past year as well as predictions for the current year and the next 10 years to come. The data of the first reported year in each edition are therefore state of the art values of technical parameters and status quo values for others. In [42] we reviewed for the first time the forecast quality of several technical parameters like the amount of remaining silver of a c-Si cell and the as-cut wafer thickness of c-Si wafers.
Saving silver in cell manufacturing is important as silver is the costliest non-silicon material in the c-Si PV value chain and a resource used not only by PV but also by other industries. The dependency on the world market requires continuous reduction of silver consumption. Reduced usage of silver will be mandatory to stay competitive.

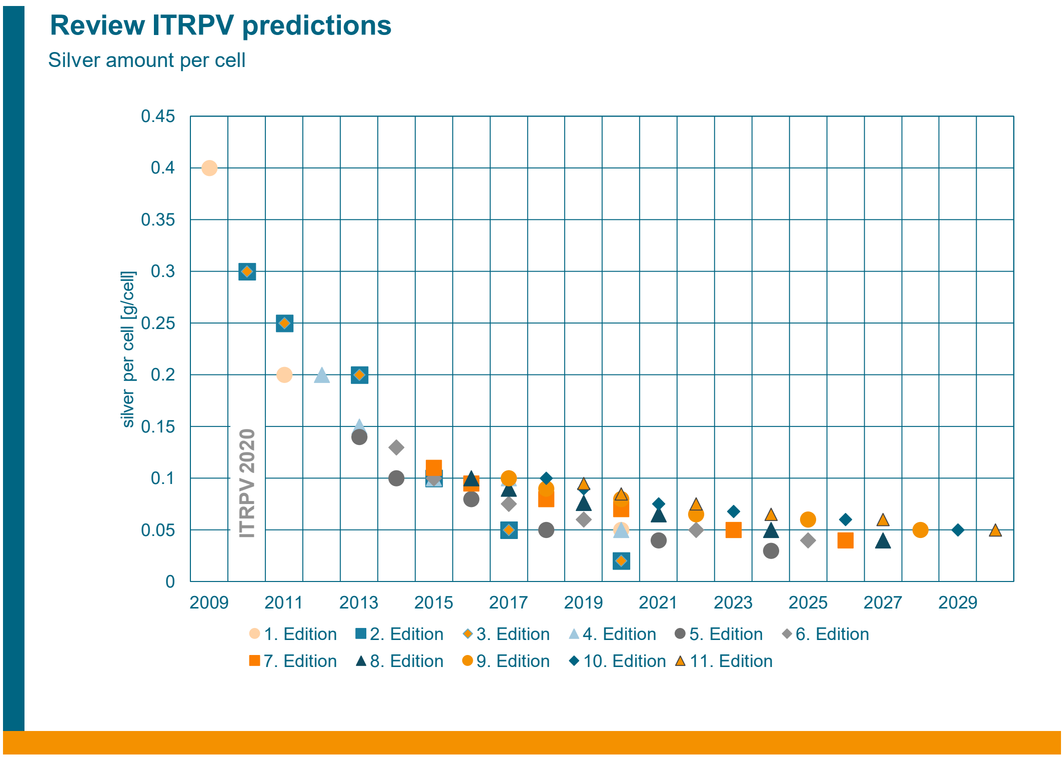


Fig. 89: Predicted trend of remaining silver per cell - predictions of ITRPV editions.

Fig. 89 shows that silver reduction - including the data of the 11th edition - has been predicted quite well since the 1st edition. Realizing less than 100 mg of remaining silver took longer than expected, but a further reduction is ongoing.

The reduction of finger width at the cell front side is following the predictions quite precise as shown in Fig. 90. Both trends emphasize that cost saving activities have been consistently continued since the 1st edition in 2010.

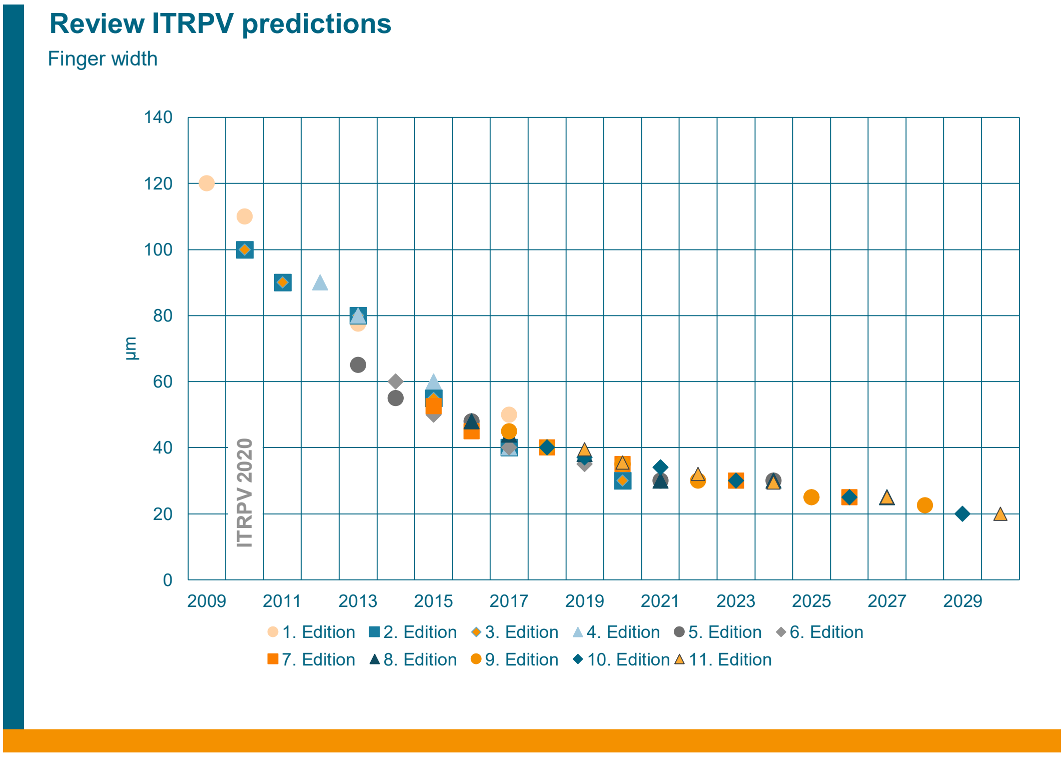


Fig. 90: Predicted trend of finger width at front side print - predictions of ITRPV editions.

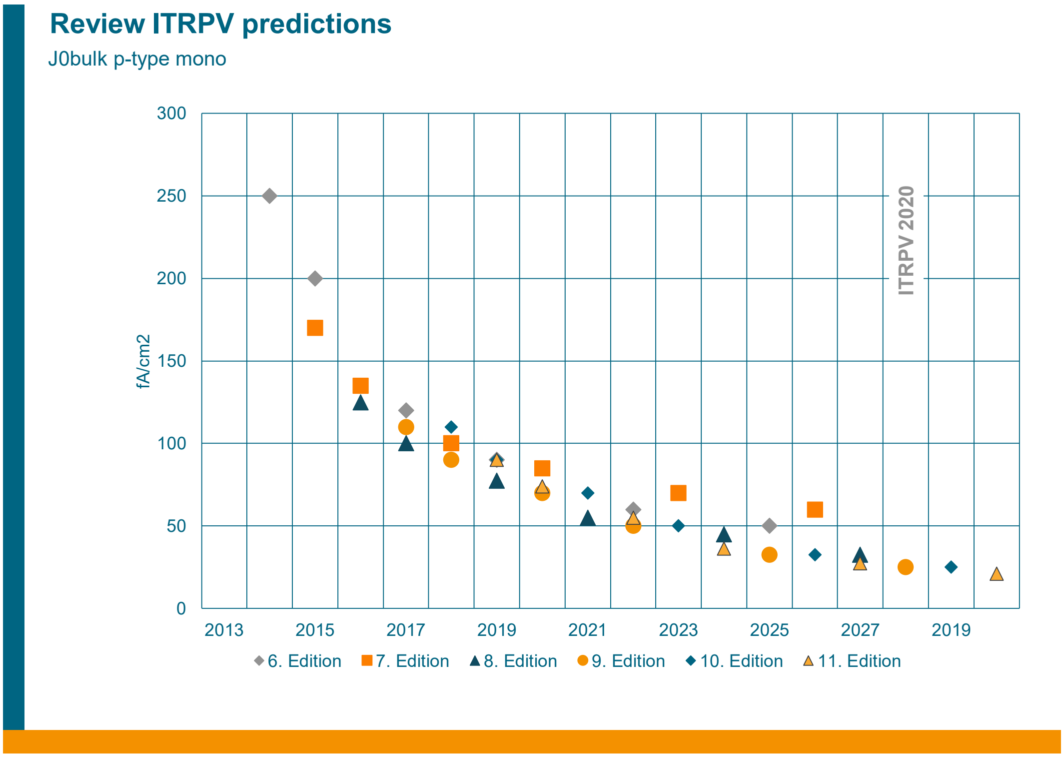


Fig. 91: Predicted trend of J0bulk for p-type mono-Si material - predictions of ITRPV editions.

The improvement of c-Si bulk is key to improve cell efficiency as discussed in chapter 6.2. Fig. 91 shows that the required J0bulk improvements of p-type mono-Si material met quite well.

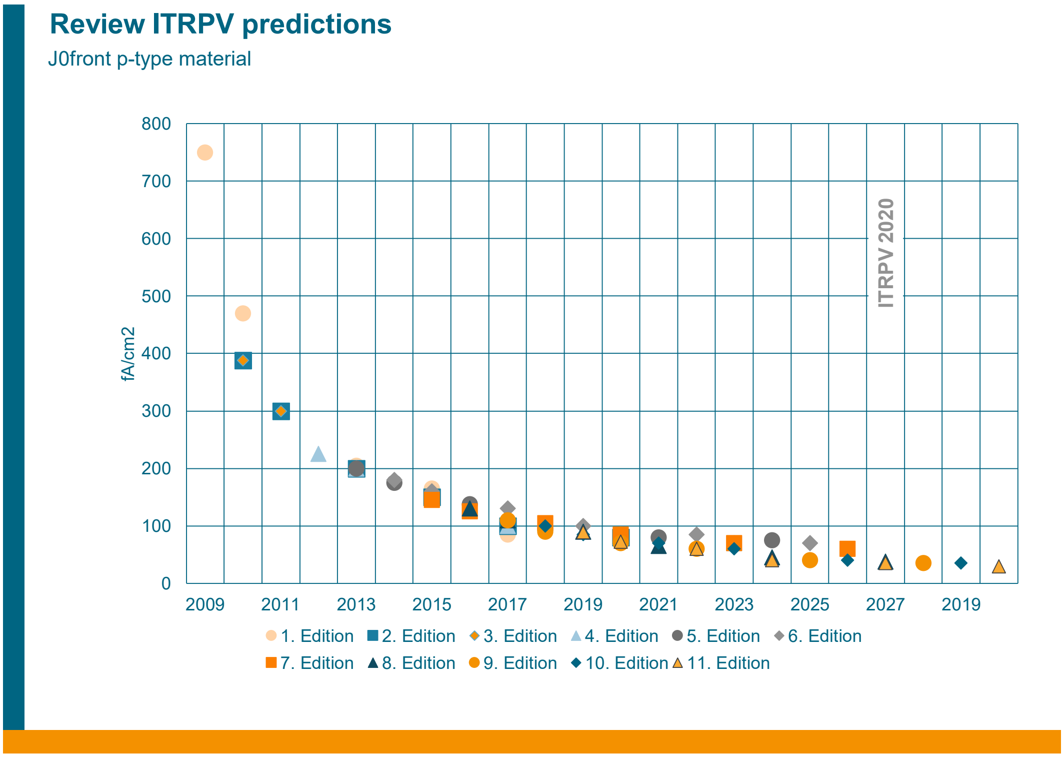


Fig. 92: Predicted trend of J0front for p-type material - predictions of ITRPV editions.

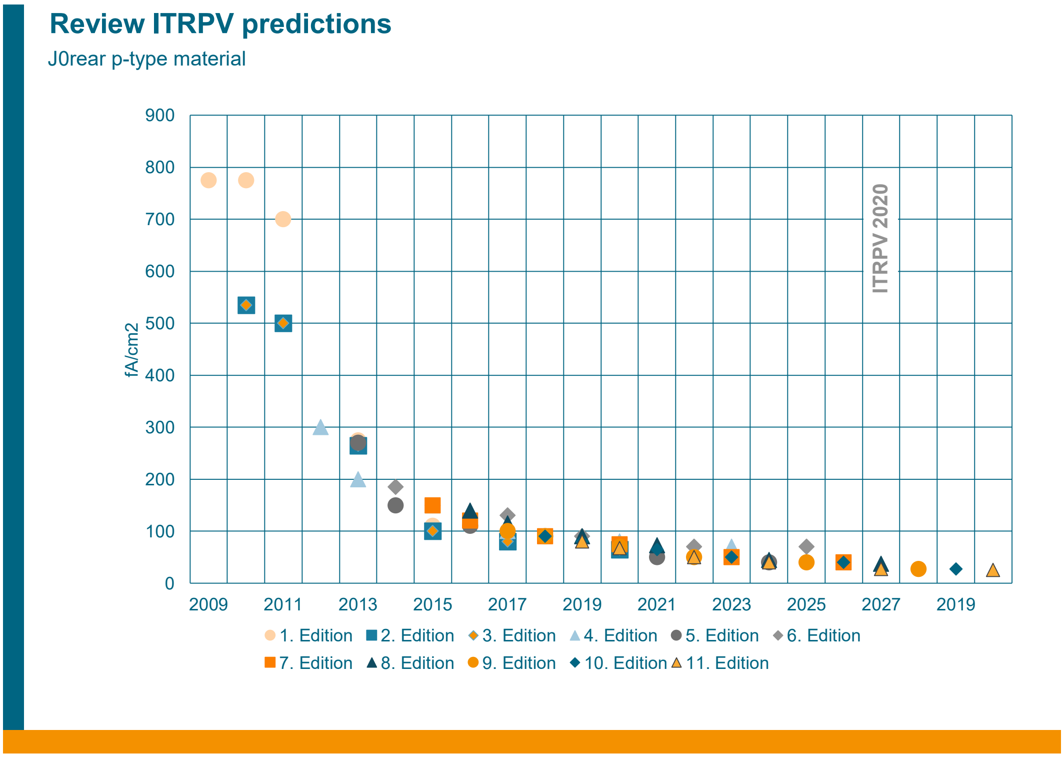


Fig. 93: Predicted trend of J0rear for p-type material - predictions of ITRPV editions.

The progress of process improvements on p-type front and rear side are shown in Fig. 92 and Fig. 93. J0front and J0rear of p-type cell concepts improved in line with ITRPV requirements.

Fig. 94 shows the prediction quality for mono-Si wafer thickness. It is clearly visible that the required thickness reduction speed was not realized at all. 180 µm remained for a long time the mainstream thickness. The reduction of silicon consumption in wafer manufacturing was realized instead by the introduction of DWS as discussed in chapter 5.2.

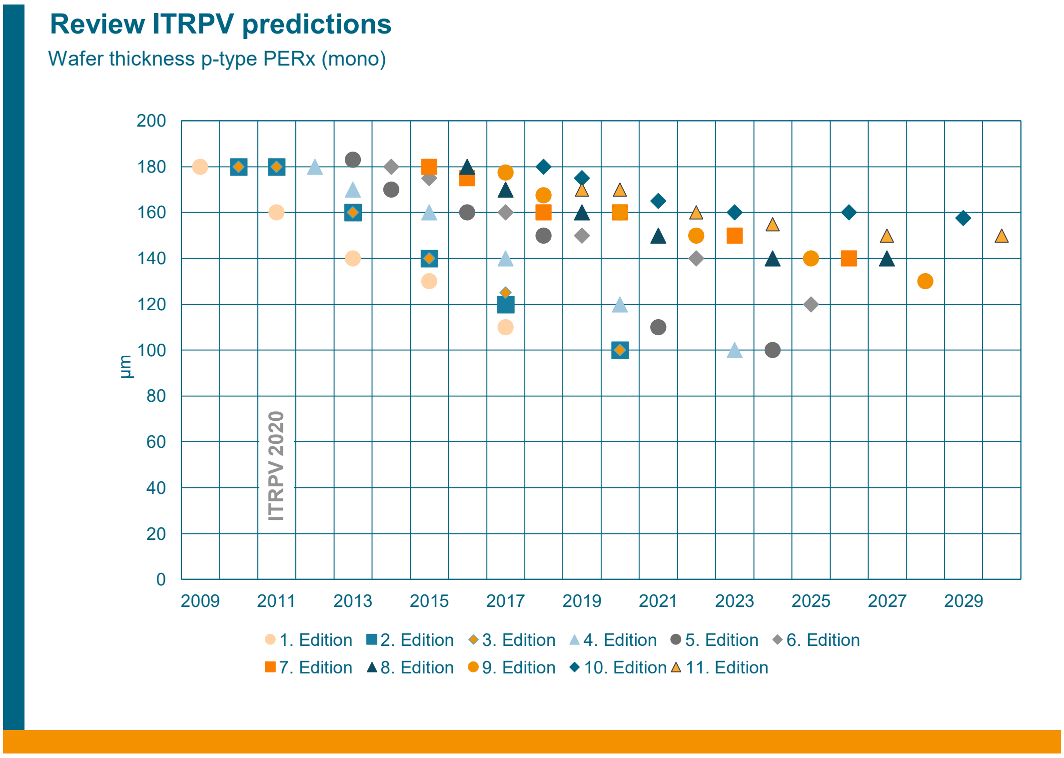


Fig. 94: Predicted trend of p-type mono-Si wafer thickness - predictions of ITRPV editions.

Nevertheless, cost savings in poly-Si were realized in parallel. In contrast to silver that is used in several industrial applications, poly-Si is a material exclusively produced and used in PV (beside some volume for the semiconductor industry). Process improvements and resulting capacity expansions enabled significant cost and corresponding price reductions.

10.4. Final remarks

We collected all data presented in this ITRPV edition at the end of 2019 from leading companies along the c-Si value chain, international PV manufacturers, PV equipment and material suppliers, PV institutes as well as PV service providers, listed in the Acknowledgment. Plans call for this information to be updated annually. The topics discussed require cooperation along the PV value chain - between tool and material suppliers, PV manufacturers, project developers, EPC companies and end-customers. A version of this document for download, as well as information on how to get involved in roadmap activities, can be found at the following website: itrpv.vdma.org.

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